Preparation tips for the final:

A. *Equations: You need to know how to derive them and how to use them*
B. *Figures: You need to understand the circuits shown*
C. *Questions will be* ***<u>only</u>*** *from the textbook and homework*
D. *The final will include all that we have discussed this semester. Review what is already posted for the midterm. This is a list of equations, figures, tables, and examples for the portion discussed after the midterm examination.*

1. Fig. 5.17: Large-signal equivalent circuit: the π-model
2. Fig. 5.23: The transfer relation defining the “depletion” mode and the “enhancement” mode FET’s
3. Example 5.4: A typical FET circuit with proper biasing network
4. Fig. 5.34: Small-signal equivalent circuit: the pi-model
5. Fig. 5.36: Development from the π-model to the T-model; in fact, the π-model and the T-model can be translated back and forth
6. Fig. 5.39: Again, biasing a MOSFET
7. Fig. 5.40: A MOS current mirror
8. Fig. 5.41: The basic MOS current mirror
9. Fig. 5.50 and Fig. 51: The two special cases where we use a MOS to deliver non-linear two-terminal characteristics --- applications shown in Fig. 5.52 and Fig. 5.53, respectively.
10. Fig. 5.55: A CMOS logic inverter
11. Fig. 5.56: The inverter with a "high" input signal
12. Fig. 5.57: The invertor with a "low" input signal
13. Fig. 5.58: The transfer relation of a CMOS inverter
14. Exercise 5.31: Typical questions to ask about this CMOS inverter --- and the definitions of noise margin, input high, input low, etc. Basically, the equations from (5.87) to (5.96).
15. Fig. 5.59: Dynamic operation curve of the specific circuit
16. Definition of "propagation delay" --- defined in Fig. 5.59(b); note that t_{PHL} is the propagation delay from "High" to "Low" of the output
17. Equation (5.95) and (5.96), as a conclusion of the derivations of the "noise margin" voltages
18. Equation 5.97 to 5.101, and understand how to calculate the time delay in a CMOS inverter
19. Equation 5.103 and the physical meaning of it
20. Explain the operation of a "transmission gate" whose circuit is shown in Fig. 5.64 (p. 439)
21. Equations and the circuit in page 446 --- the derivation of the "unity-gain frequency"
22. Fig. 6.3: Basic operation principle of a differential pair --- the transfer characteristics
23. The derivation and the result in equation 6.17
24. The most important parameters of a differential pair is (1) voltage gain [the expressions are shown in equation (6.30) and (6.32)], (2) input resistance [equation (6.23) and (6.24)], and (3) CMRR expressed in dB.
25. Fig. 12.1: The basic concept of "positive" feedback that leads to unstable conditions
26. Equations (12.1) - (12.4) are used to define the problem better.
27. Fig. 12.19: a bistable circuit showing hysteresis
28. Fig. 12.20: another bistable circuit with the hysteresis feature in its transfer relation
29. Fig. 12.24: RC relaxation astable multivibrator

30. Fig. 12.25: Triangular and square wave generator
31. Fig. 12.28: Using 555 timer in a monostable multivibrator circuit
32. Fig. 12.29: Using the same 555 timer IC in an astable multivibrator
33. Fig. 12.33 and 12.34: How to build a superdiode using feedback + opamp
34. Example 13.1 (page 1056): go through the numbers to have a feeling how large the quantities are.
35. Fig. 13.7 repeats the information discussed in Fig. 5.59
36. Fig. 13.8 shows the general block diagram of a CMOS logic gate; Fig. 13.9 shows a few examples of pull-down networks; Fig. 13.10 shows a few examples of pull-up networks; Fig. 13.12, Fig. 13.13, Fig. 13.14 and Fig. 13.15 further show two CMOS logic gate examples
37. Page 1065: the bottom has an important summary of “the synthesis method”
38. Section 13.5: the concept of using pass-transistors to build logic gates --- the advantage and the disavantages of this design concept
39. Fig. 13.30, Fig. 13.31 and Fig. 13.32: examples of pass-transistor logic
40. Section 13.6: the need, for certain logic families, for "dynamic" operation
41. For all of the memory elements, make sure that you understand and memorize the definitions and the differences between them.
42. Section 13.7: latch --- Fig. 13.38 (a), (b) and (c) and the latch's operation (the concept is important for both DRAM and SRAM)
43. Fig. 13.39: A variation of FF is called SR-FF and the purpose is?
44. Fig. 13.40: A CMOS implementation of a SR-FF
45. Fig. 13.42: A CMOS implementation of a clocked SR-FF
46. Fig. 13.44, Fig. 13.45, Fig. 13.47, Fig. 13.52 and Fig. 13.53. In particular, the ring oscillator's operating principle on page 1112
47. SRAM: Fig. 13.55 and the basic operating principle of a CMOS SRAM
48. DRAM: Fig. 13.58 and equations 13.58 to 13.61 --- be sure that you can calculate the voltage change at the bit line
49. Page 1125: the “Sensing amplifier” plus the precharge/equalization circuit design; the standard version is shown in Fig. 13.60
50. Fig. 13.61: the voltage on the bit line gradually develops as the feedback loop pins the voltage to the extremes; example 13.7 put in real numbers
51. Fig. 13.62 shows the use of a dummy cell for reading the data in a DRAM cell
52. Fig. 13.63 shows a NOR decoder design
53. EEPROM: structure shown in Fig. 13.67; operating principle, and Fig. 13.68 shows the electrical characteristics
54. Section 14.1: Why bipolar is slow due to the “minority carrier lifetime” problem, and how to solve this problem?
55. RTL, DTL, TTL, totem-pole output stage
56. Fig. 14.20 and Fig. 14.22: TTL inverter
57. Section 14.6 on ECL: ECL is the fastest logic family, but why is that?
58. Fig. 14.34: Typical wiring trick to handle a fast pulse through long (tens of feets) distance