Evaluating the Vulnerabilities of Digital Systems

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Electrical & Computer Engineering
University of Maryland

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The Problems

DATA INPUT/OUTPUT

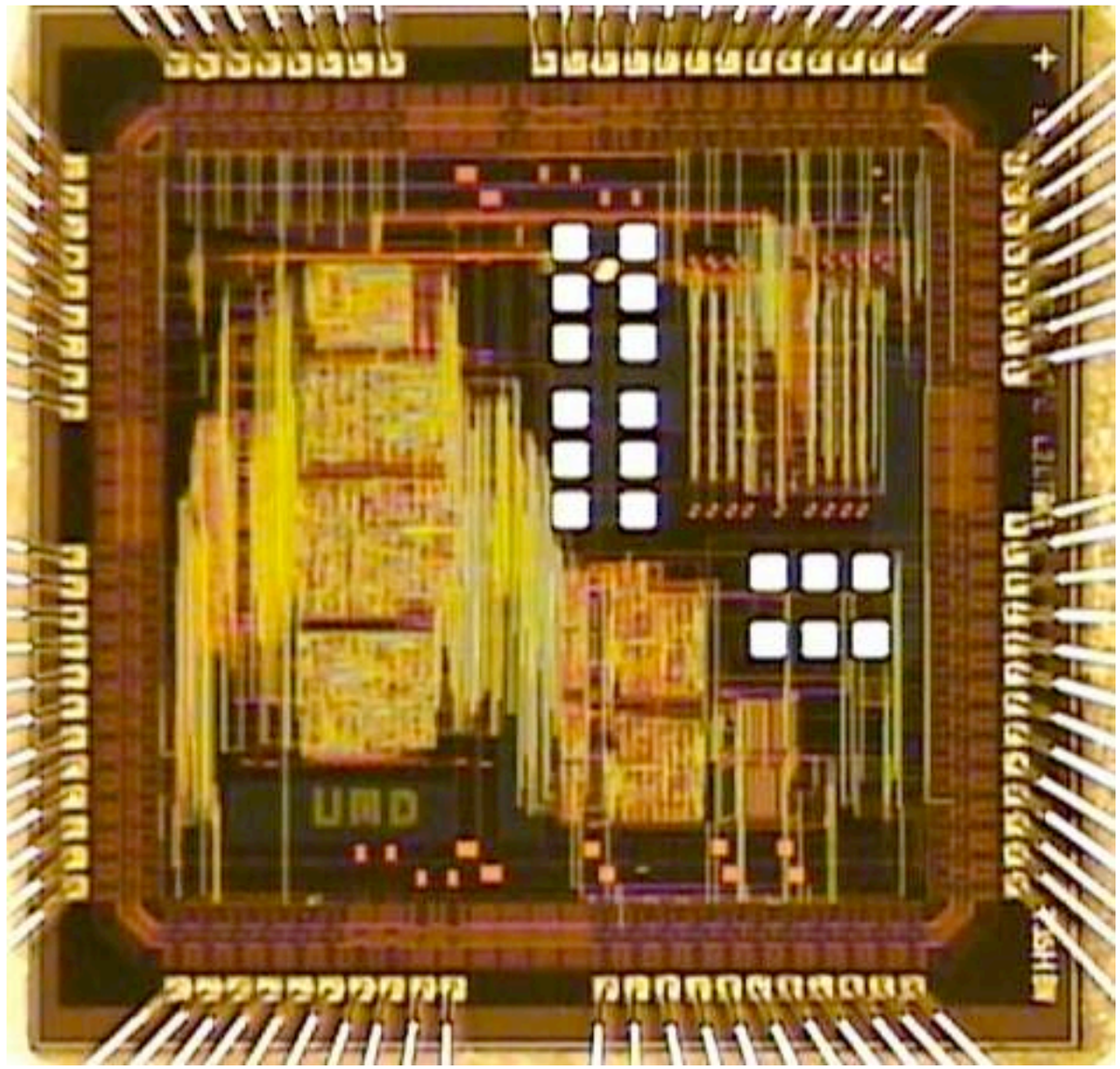
CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING

DATA

CLK



3.3V →

0V →

The Problems

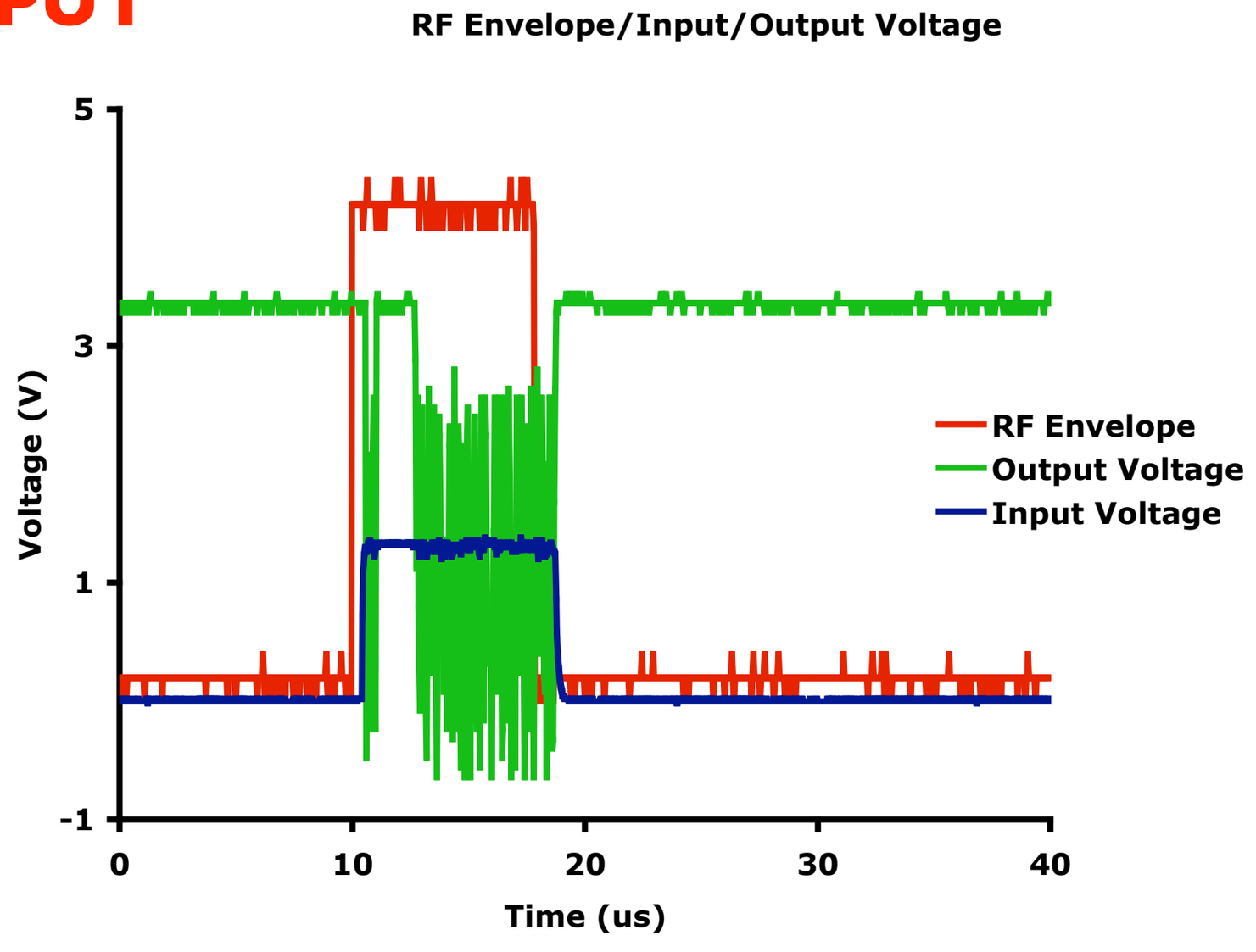
DATA INPUT/OUTPUT

- Data corrupted irreparably and silently

CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING



The Problems

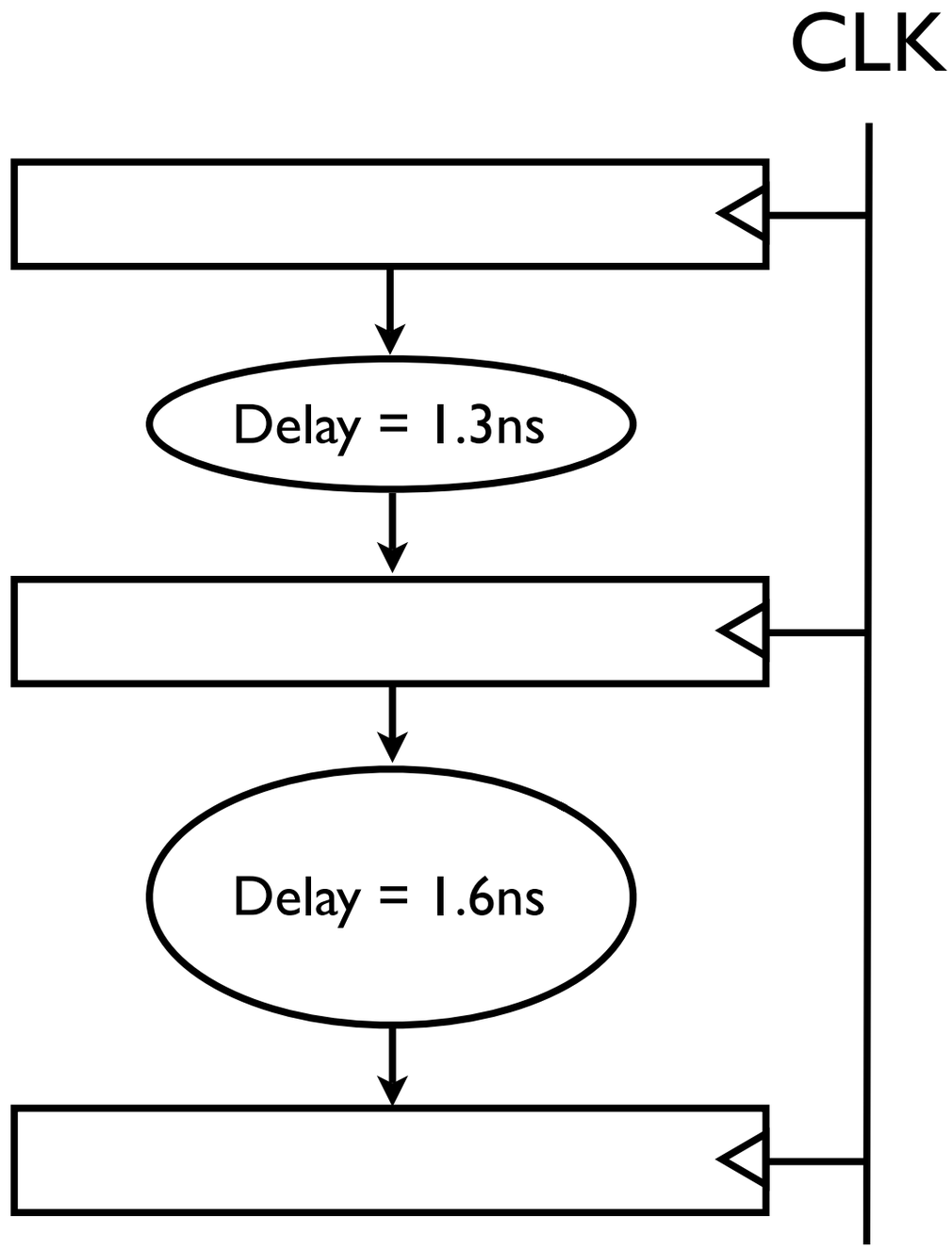
DATA INPUT/OUTPUT

CLOCK INPUT

- The Achilles' Heel of synchronous systems

GROUND PLANES

ON-CHIP COUPLING



The Problems

DATA INPUT/OUTPUT

CLOCK INPUT

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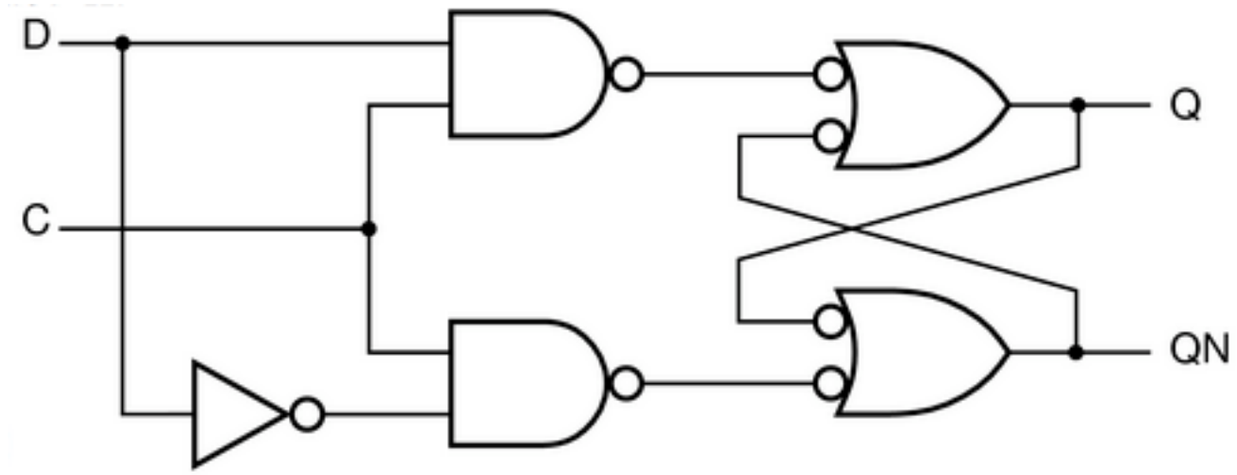
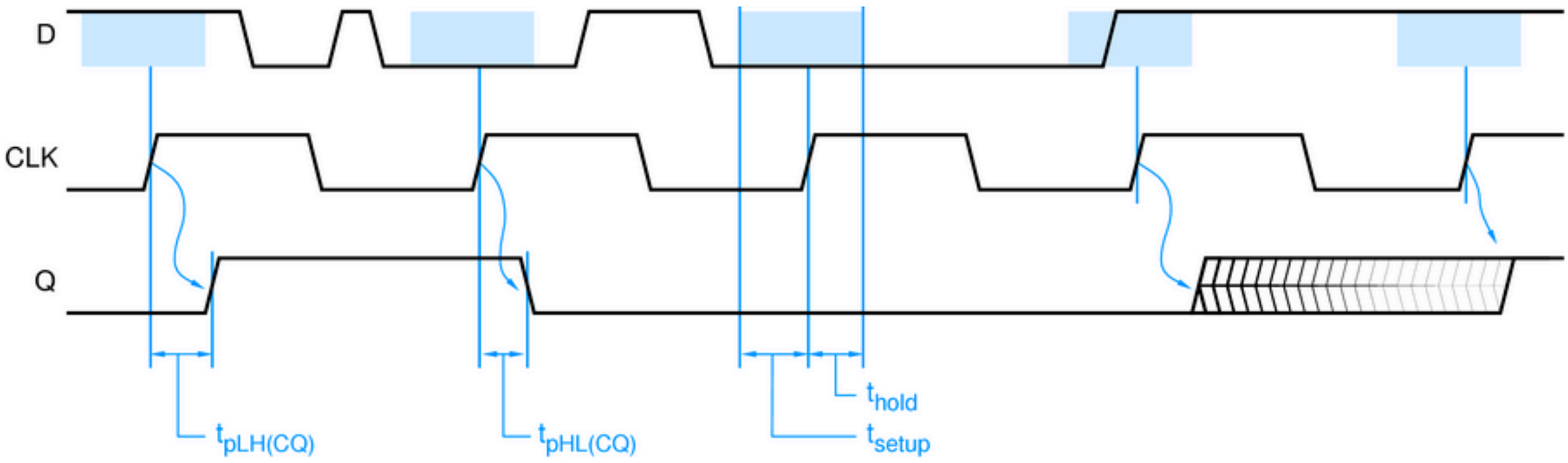




The Problems

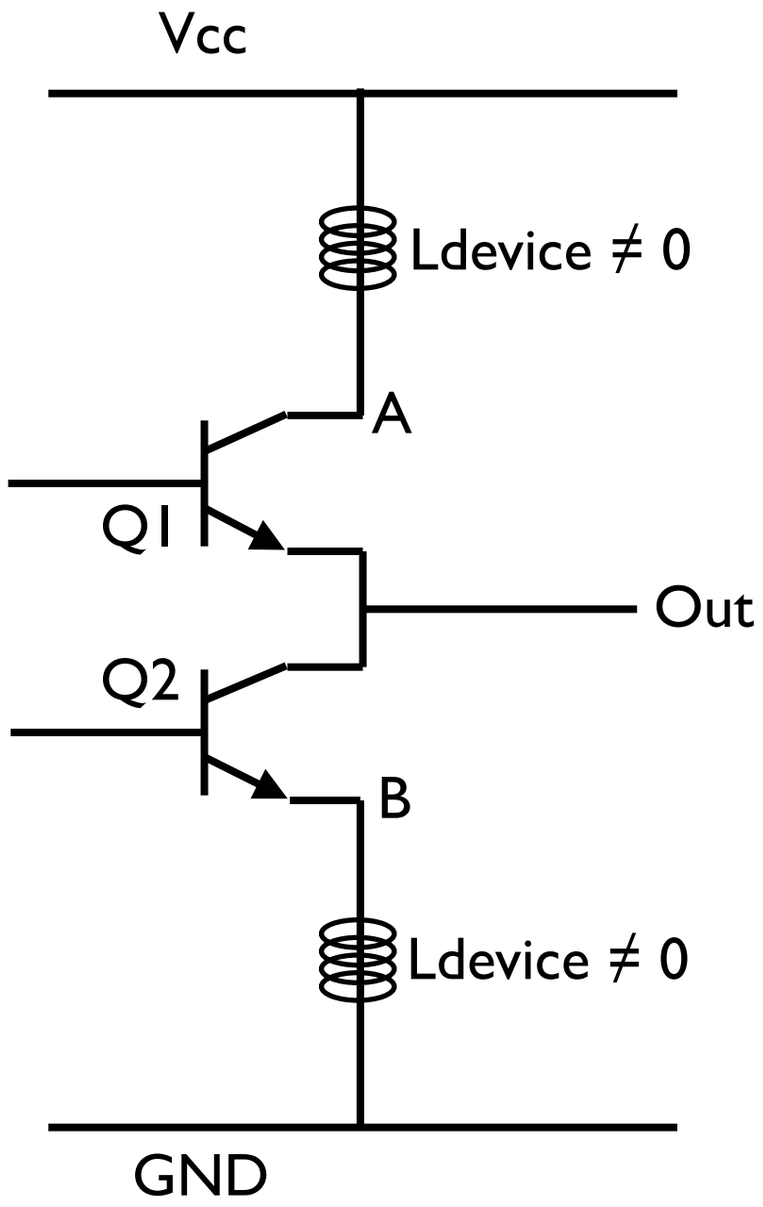
DATA INPUT/OUTPUT

CLOCK INPUT

GROUND PLANES

- Ground bounce effects change timing

ON-CHIP COUPLING



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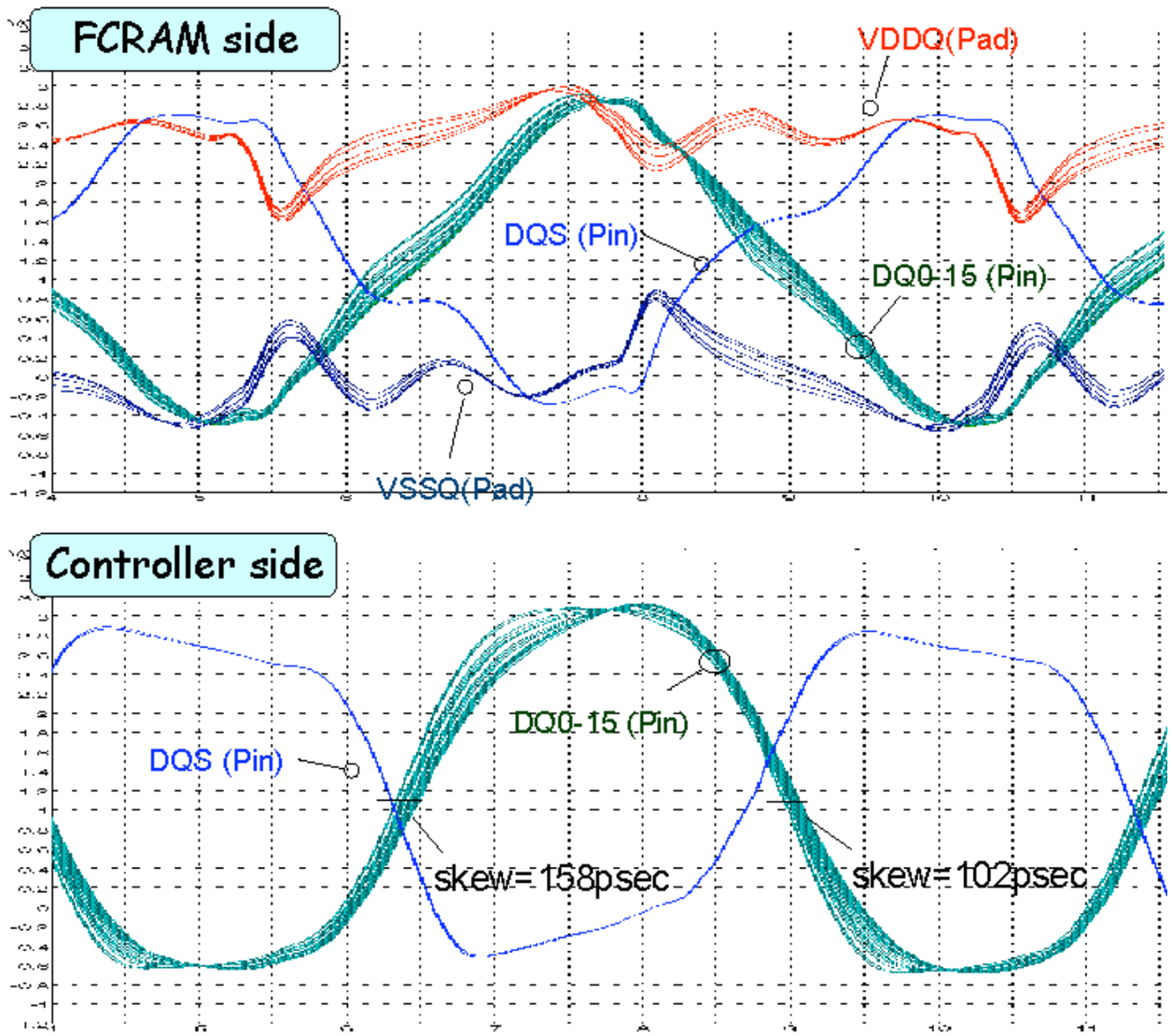


The Problems

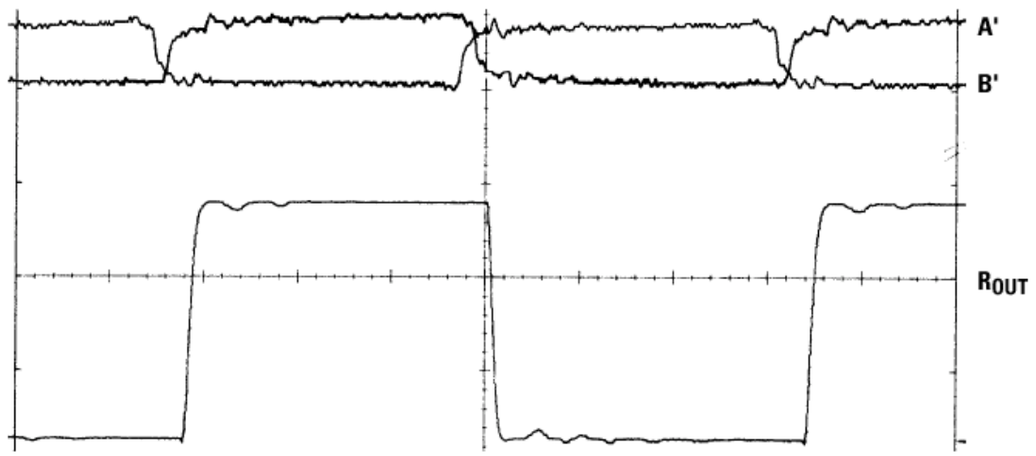
DATA INPUT/OUTPUT

CLOCK INPUT

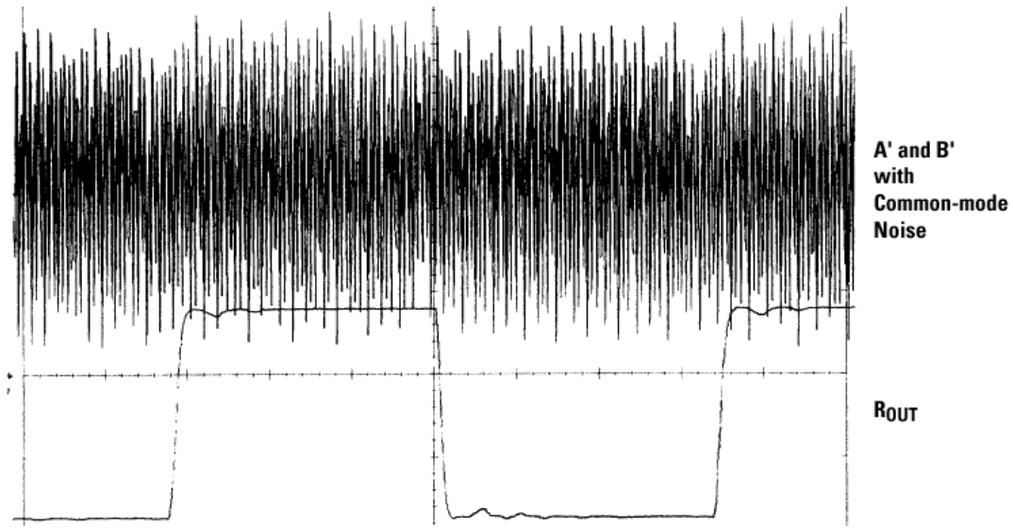
GROUND PLANES

ON-CHIP COUPLING

- Direct coupling avoids potential mitigation



Reference waveform showing LVDS signal and receiver output.



Coupled common-mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.

Differential Signaling

The Problems

DATA INPUT/OUTPUT

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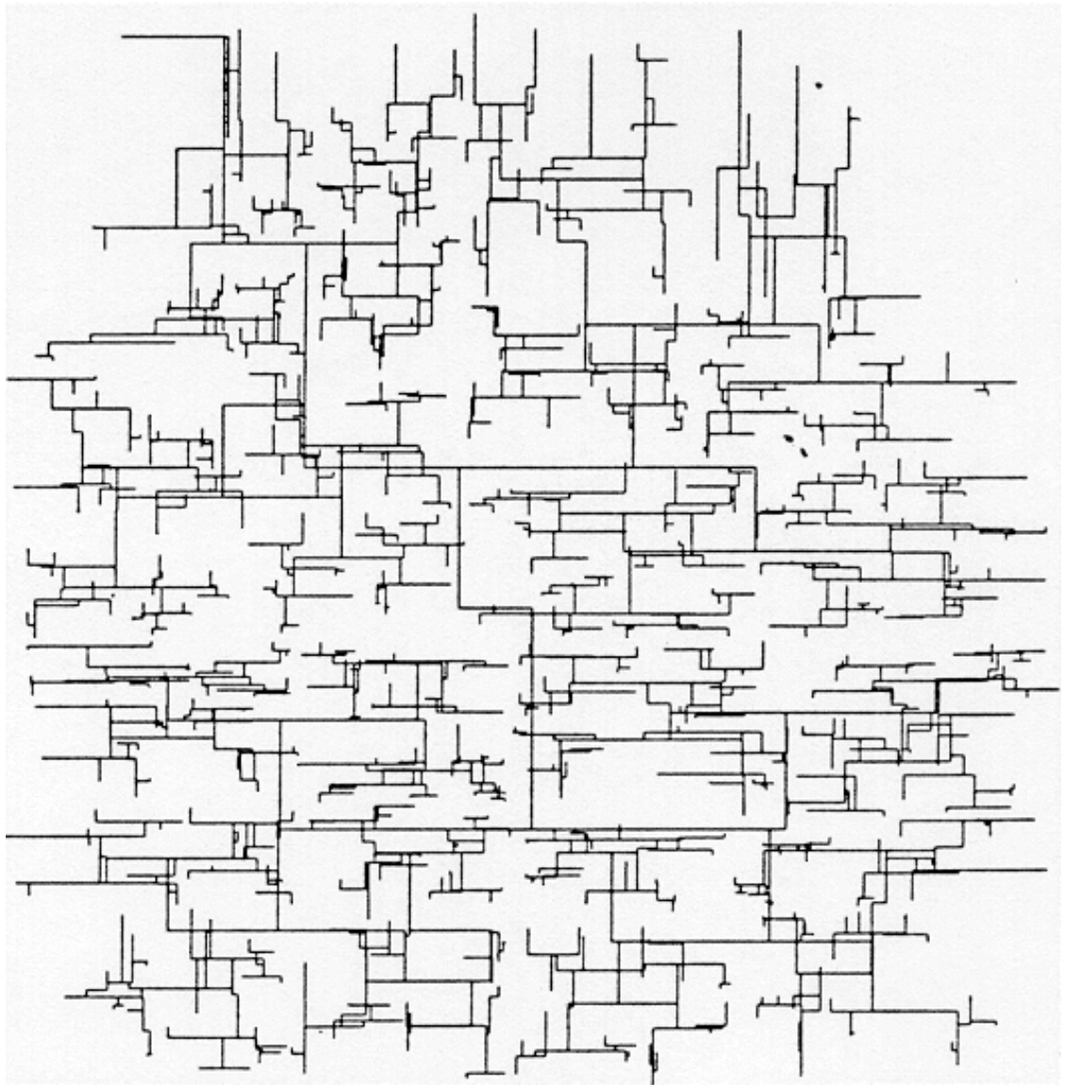


Clock Tree

The Problems

DATA INPUT/OUTPUT — **Timing** and **Levels** Matter

CLOCK INPUT — Only **Edges** Matter

GROUND PLANES — **Any Levels** Can Be Problematic

ON-CHIP COUPLING — Need to Quantify

Recent Work

DATA INPUT/OUTPUT

CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING

Recent Work

DATA INPUT/OUTPUT

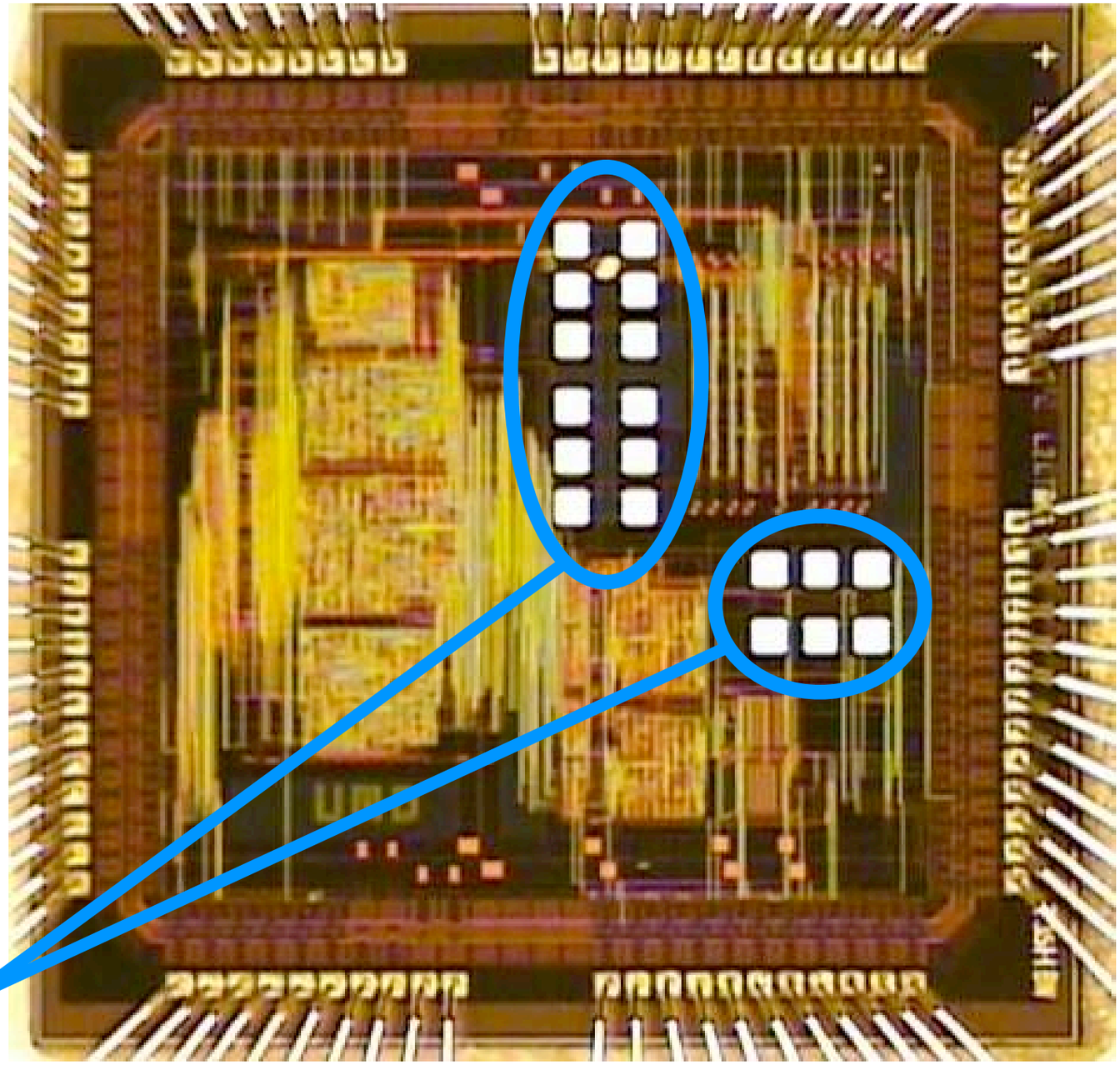
- Extremely accurate measurements of ESD

CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING

Latest chip design
for Rodgers & Firestone



Custom-designed on-chip pads
to accommodate input probes

Recent Work

DATA INPUT/OUTPUT

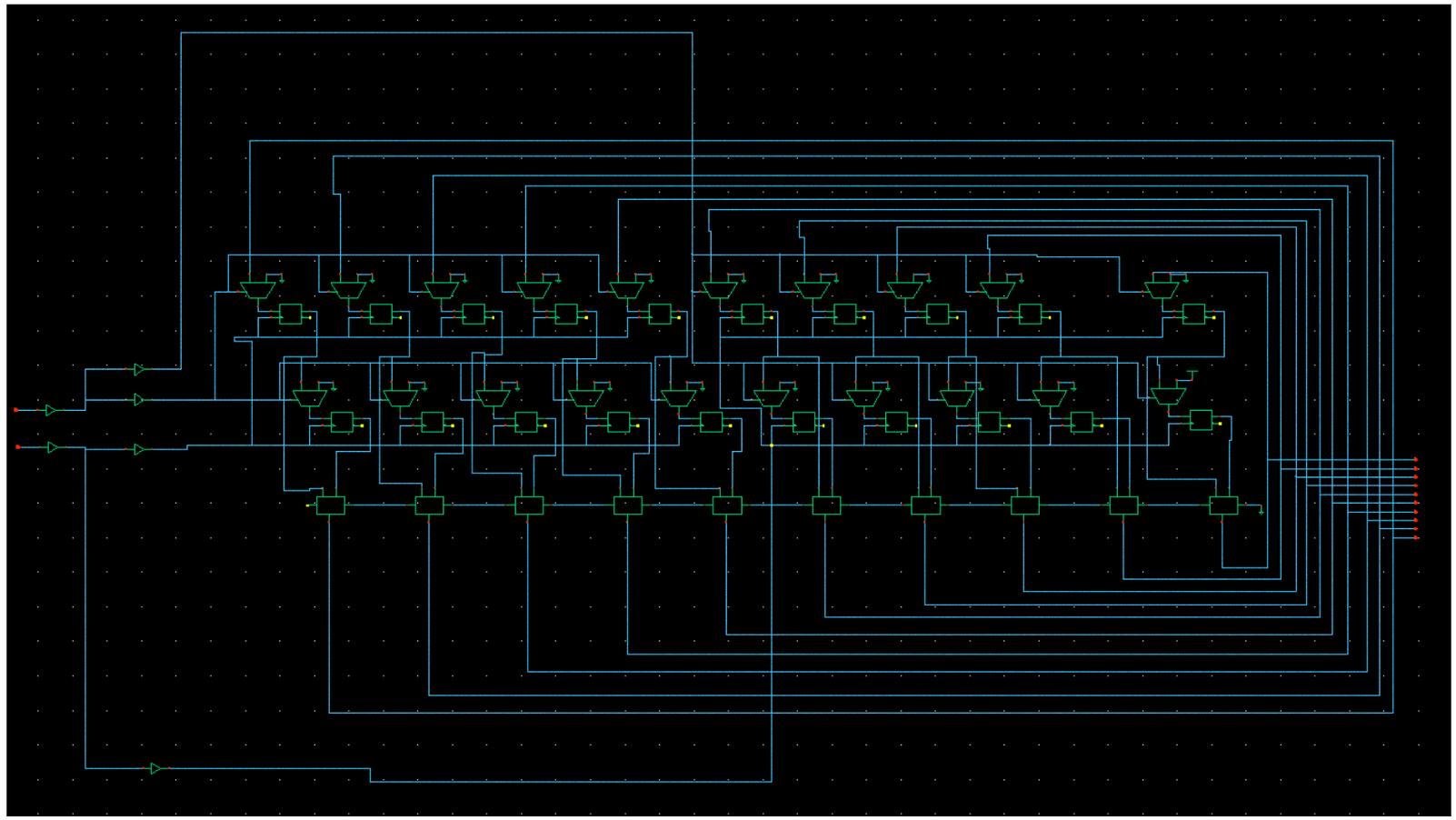
CLOCK INPUT

- Characterize the susceptibility of CLK

GROUND PLANES

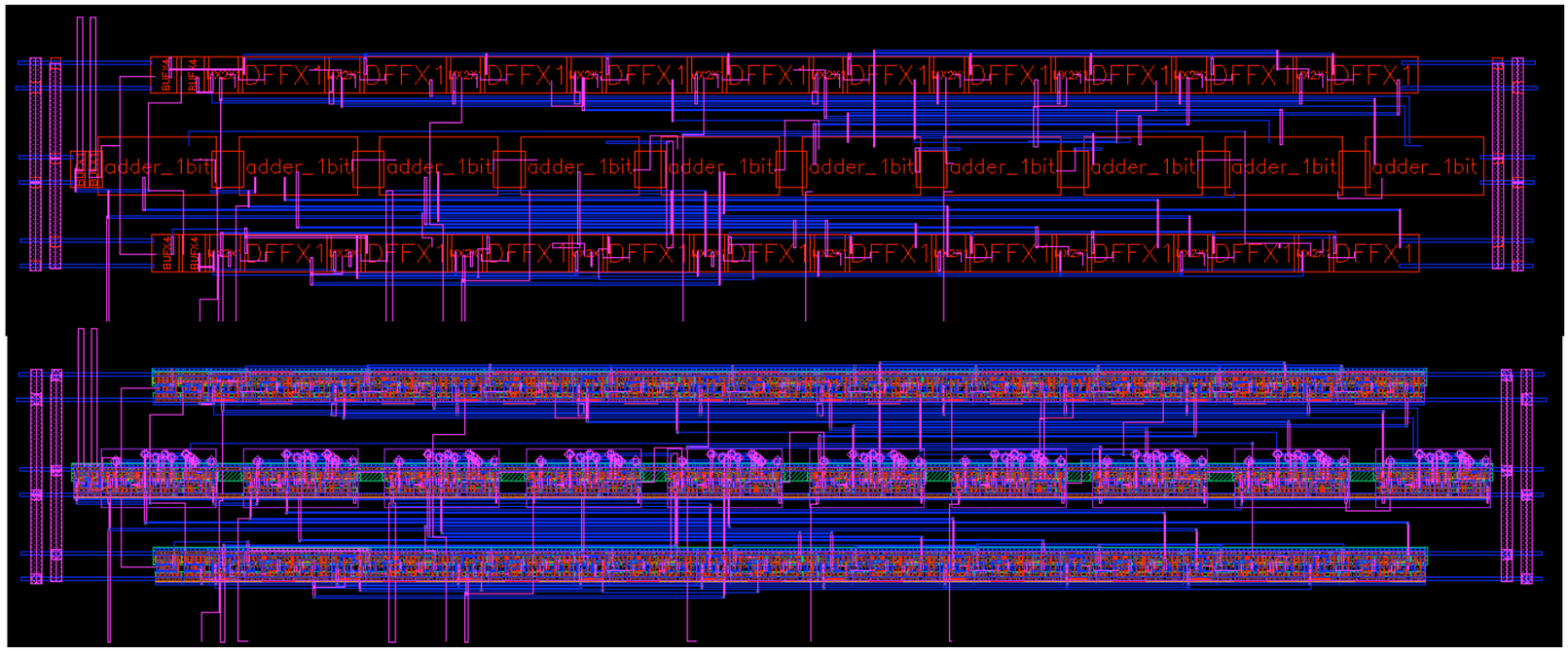
ON-CHIP COUPLING

8-bit Ripple Counter



Recent Work

8-bit Ripple Counter



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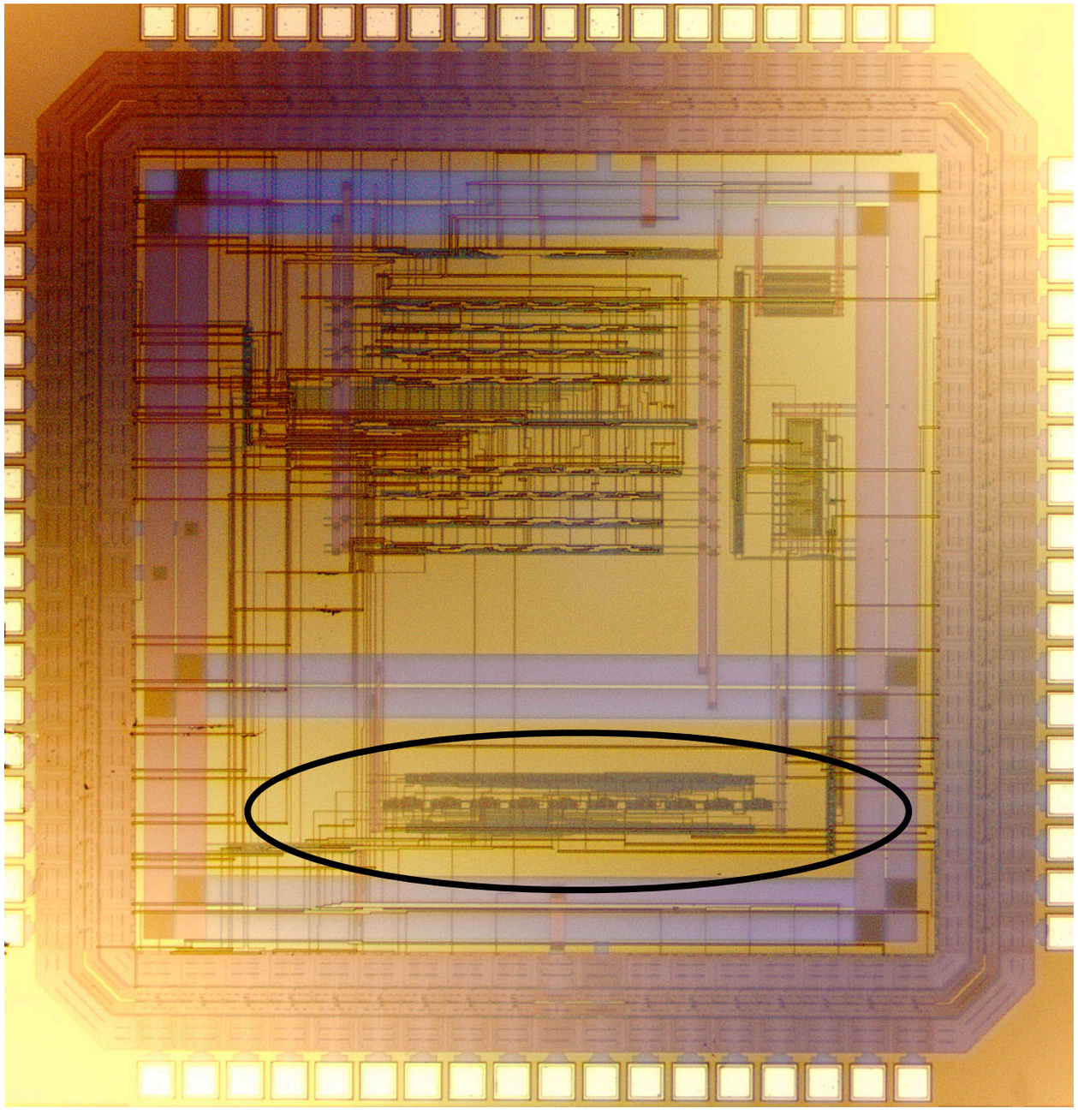

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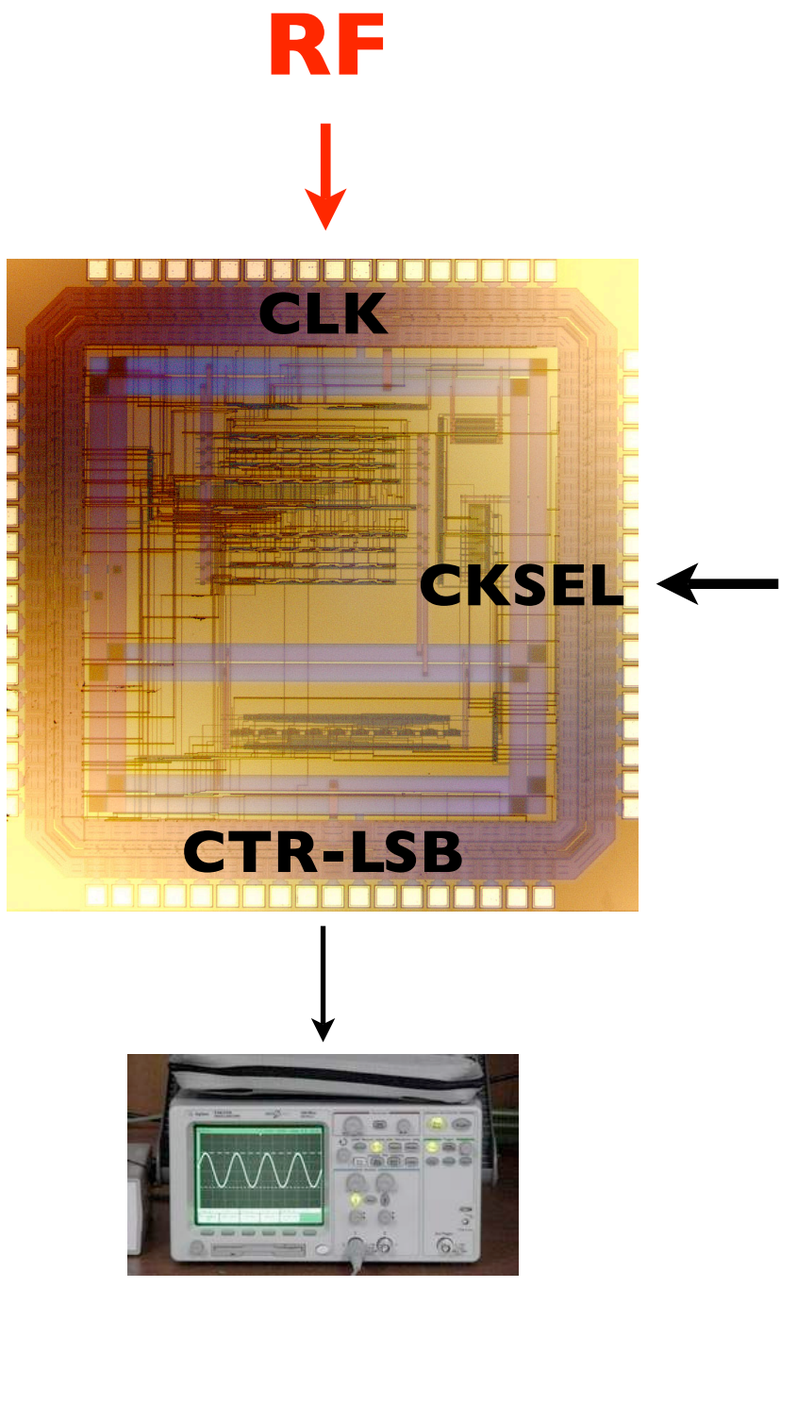

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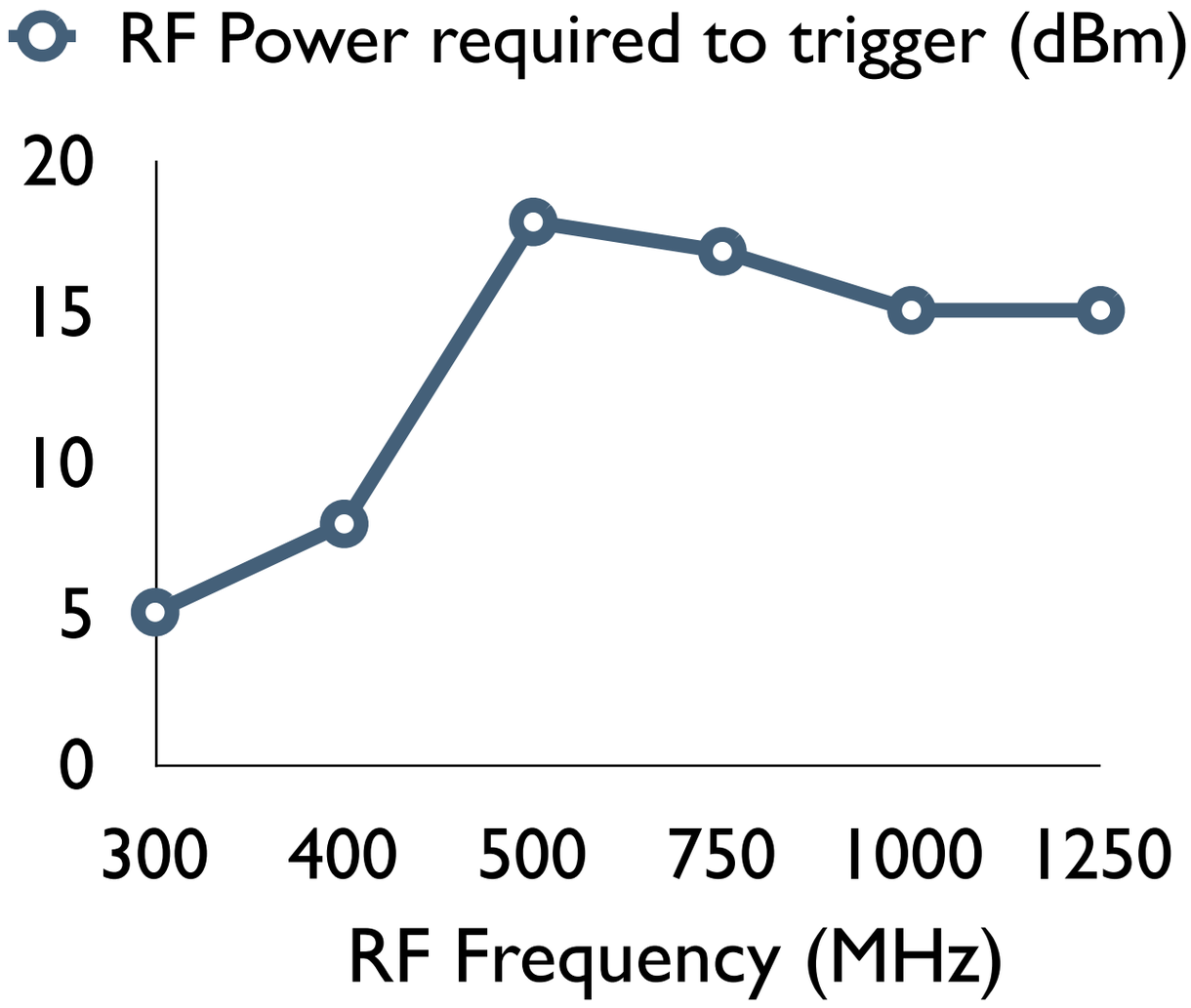

Power/Voltage-vs-Frequency
(min. to cause transitions)

Rec

DATA INPUT/OUTPUT

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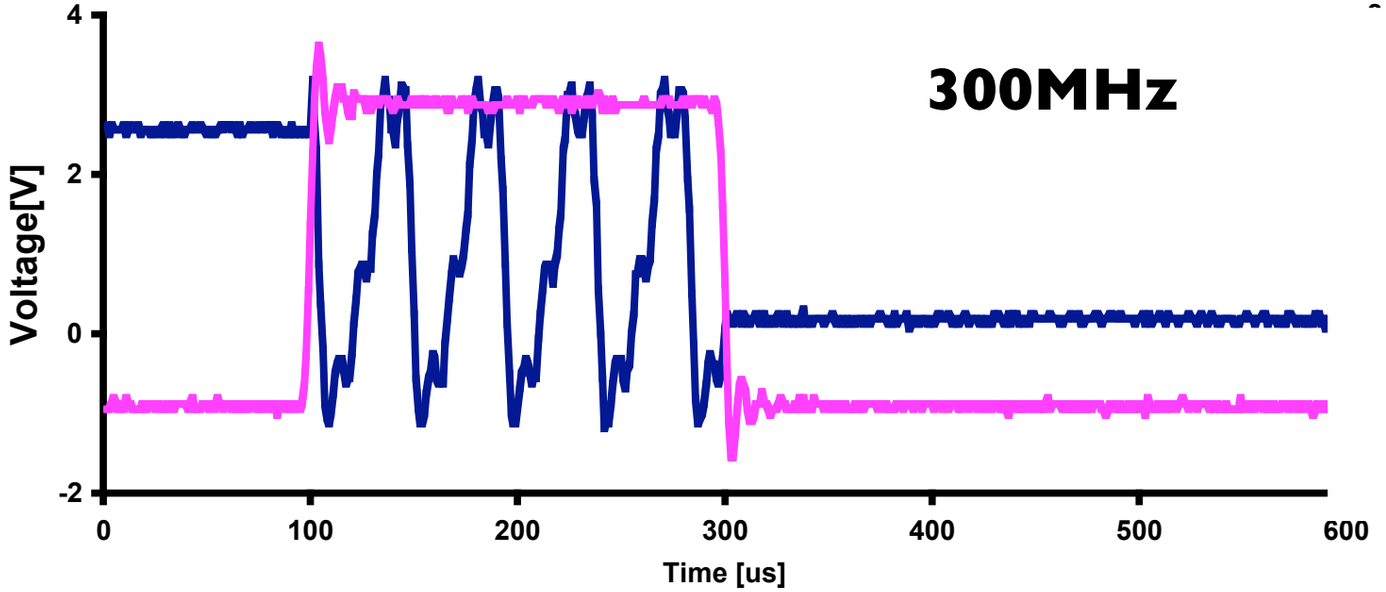

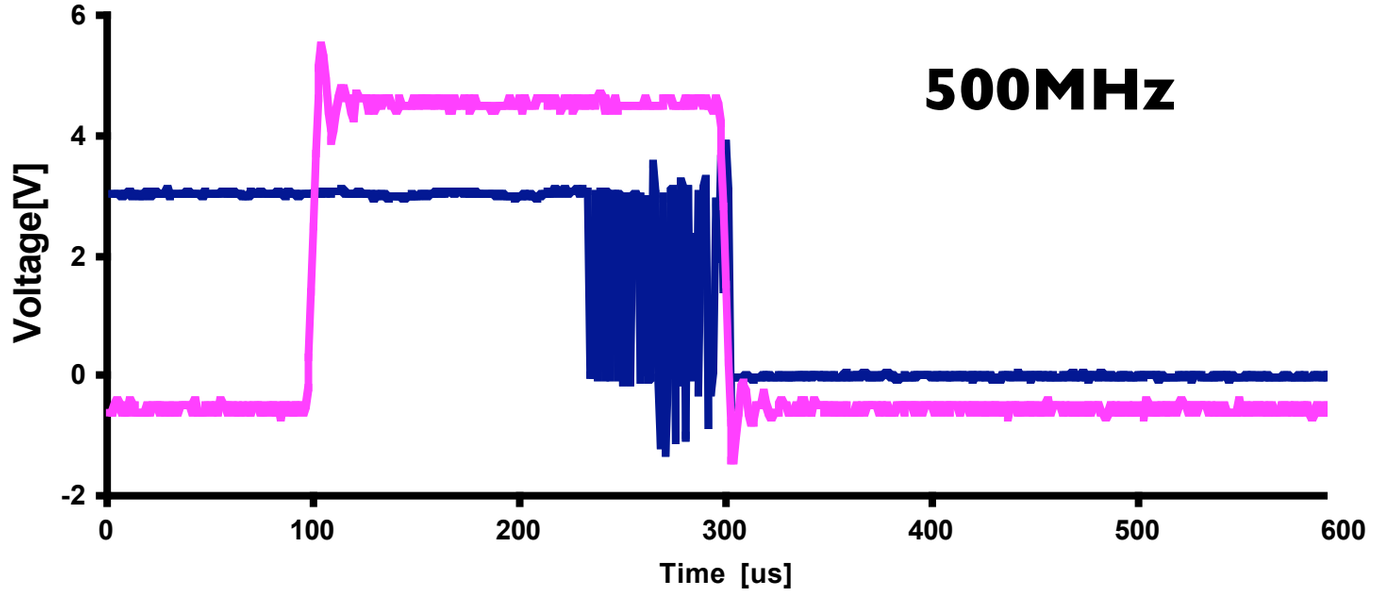

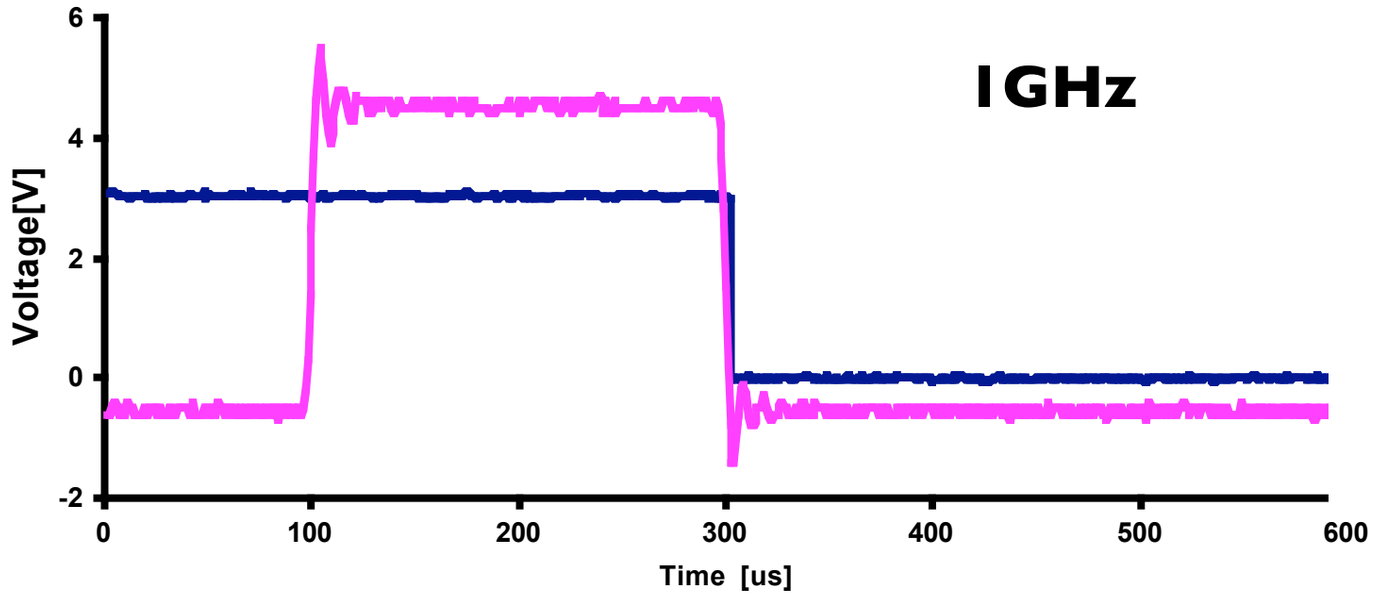

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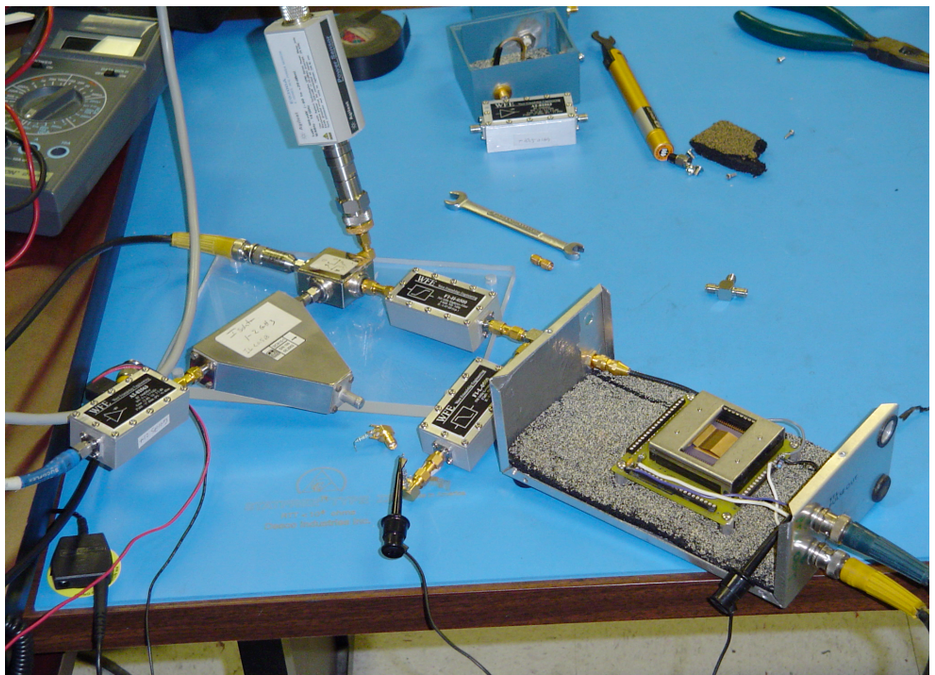
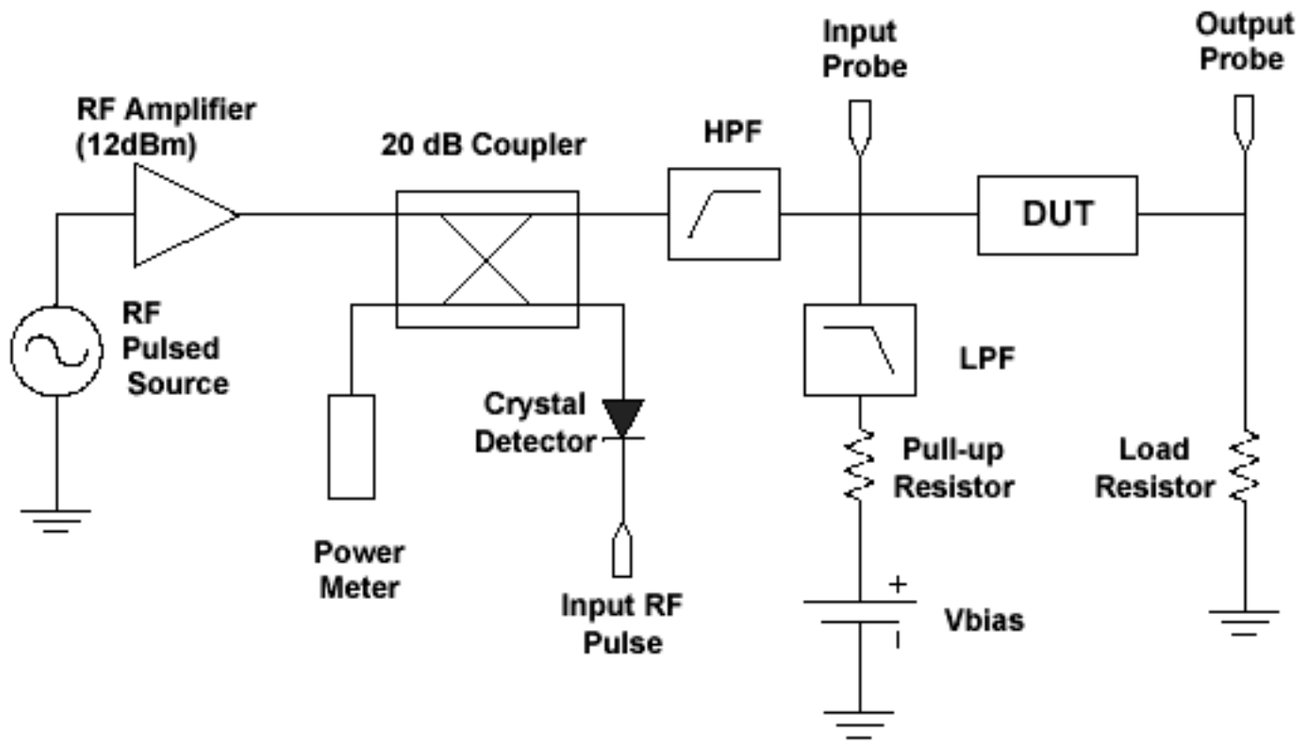


Experimental set-up
for RF direct injection studies



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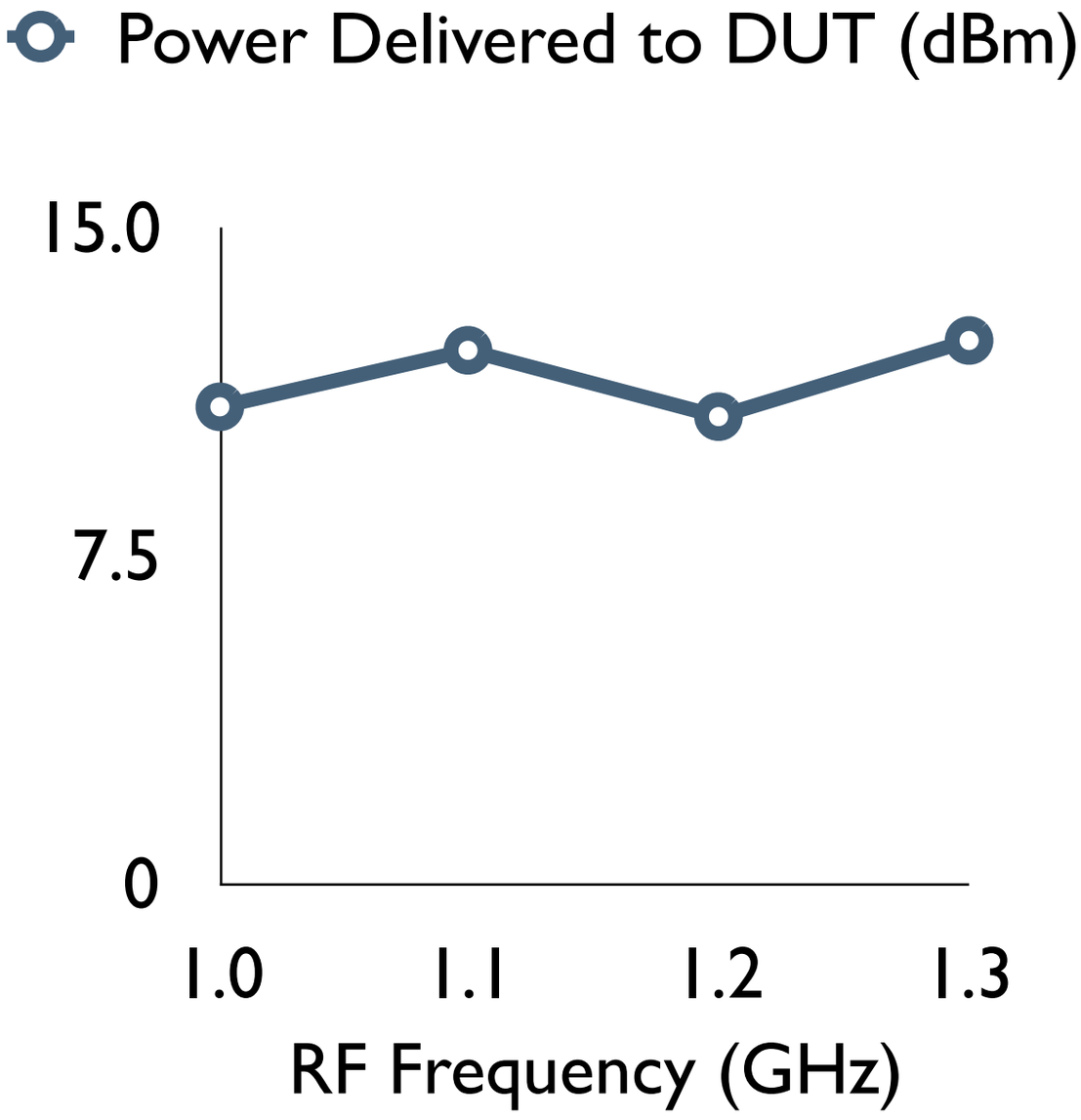

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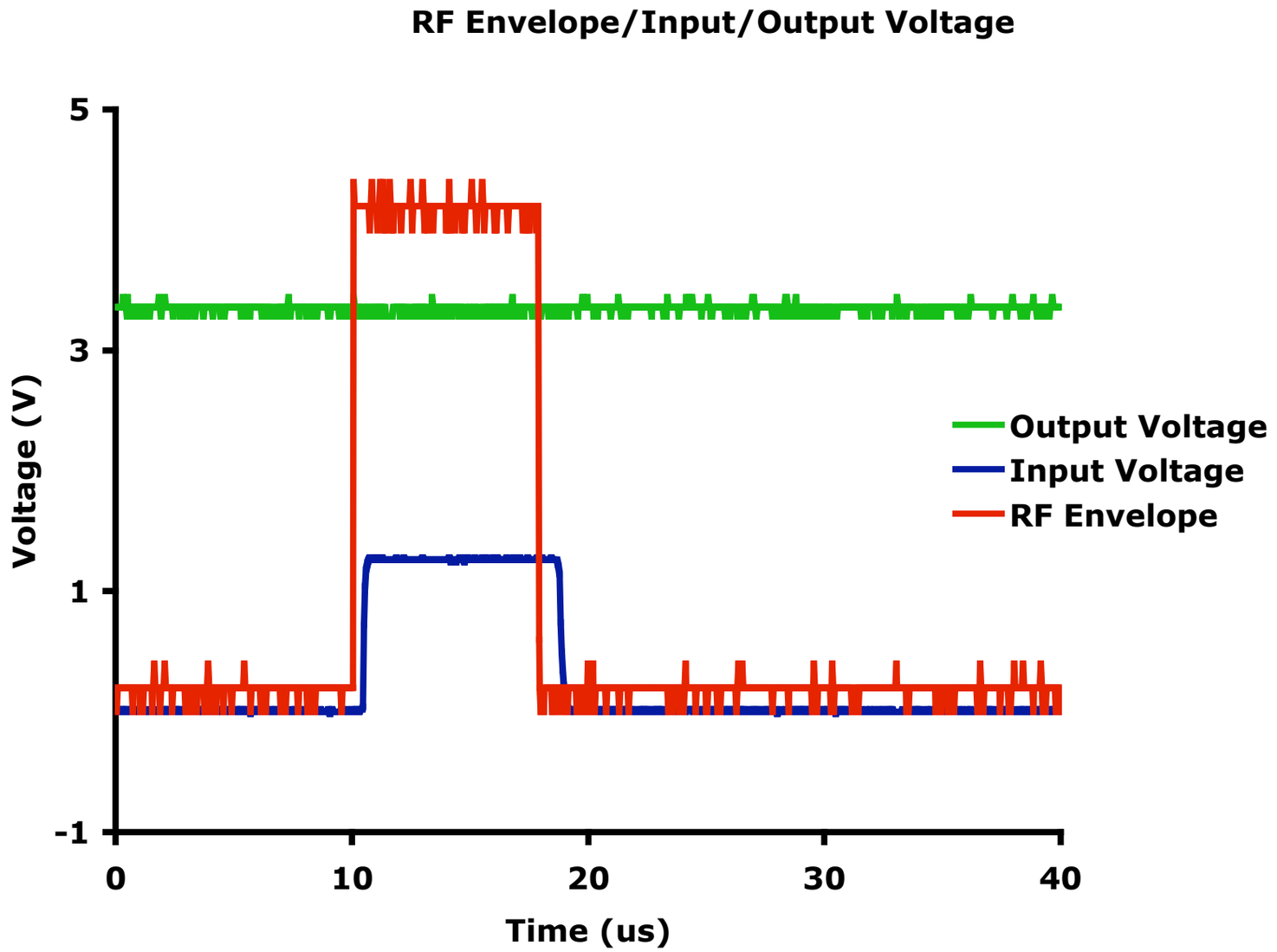

1GHz, ~20dBm RF

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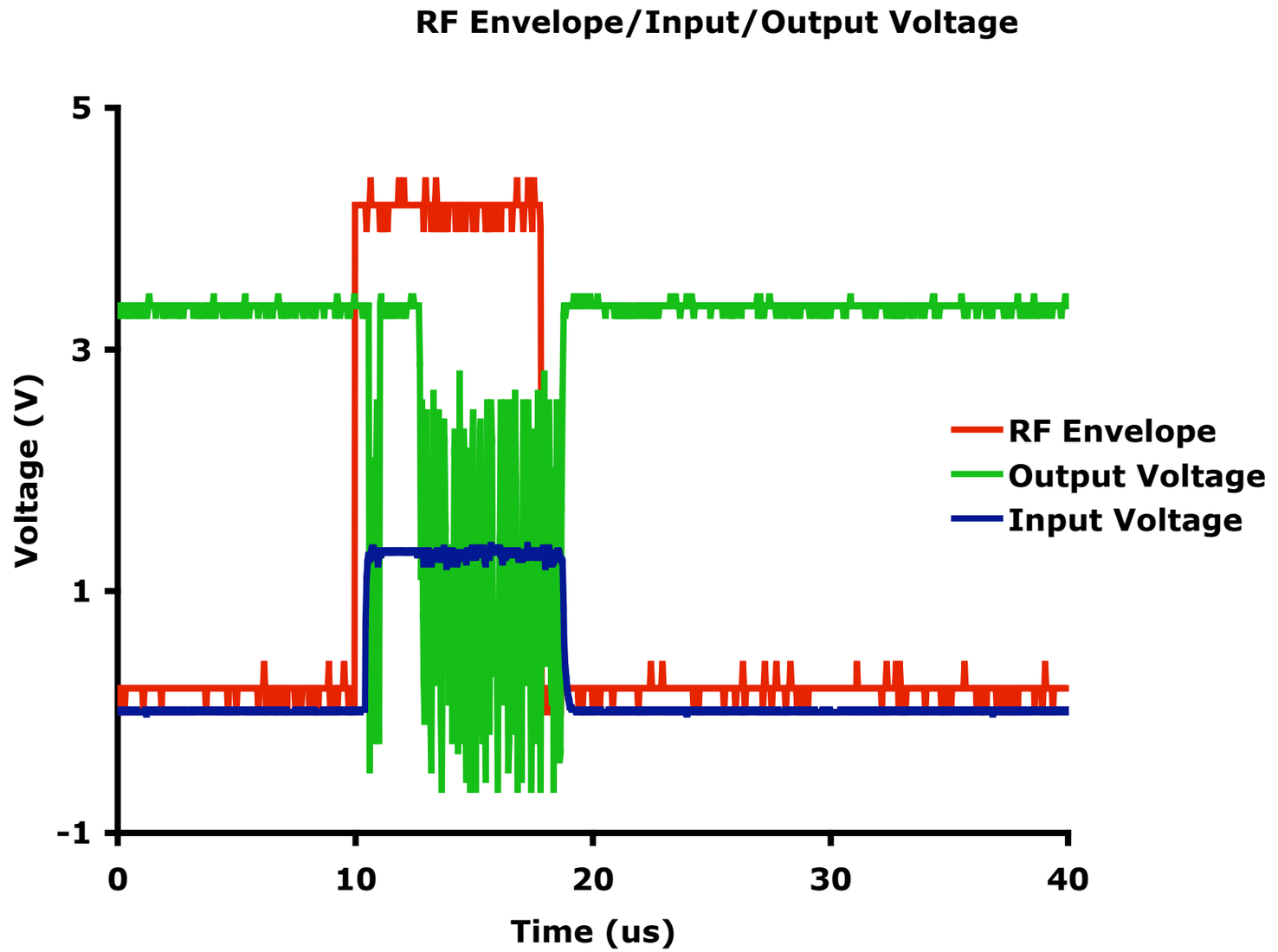

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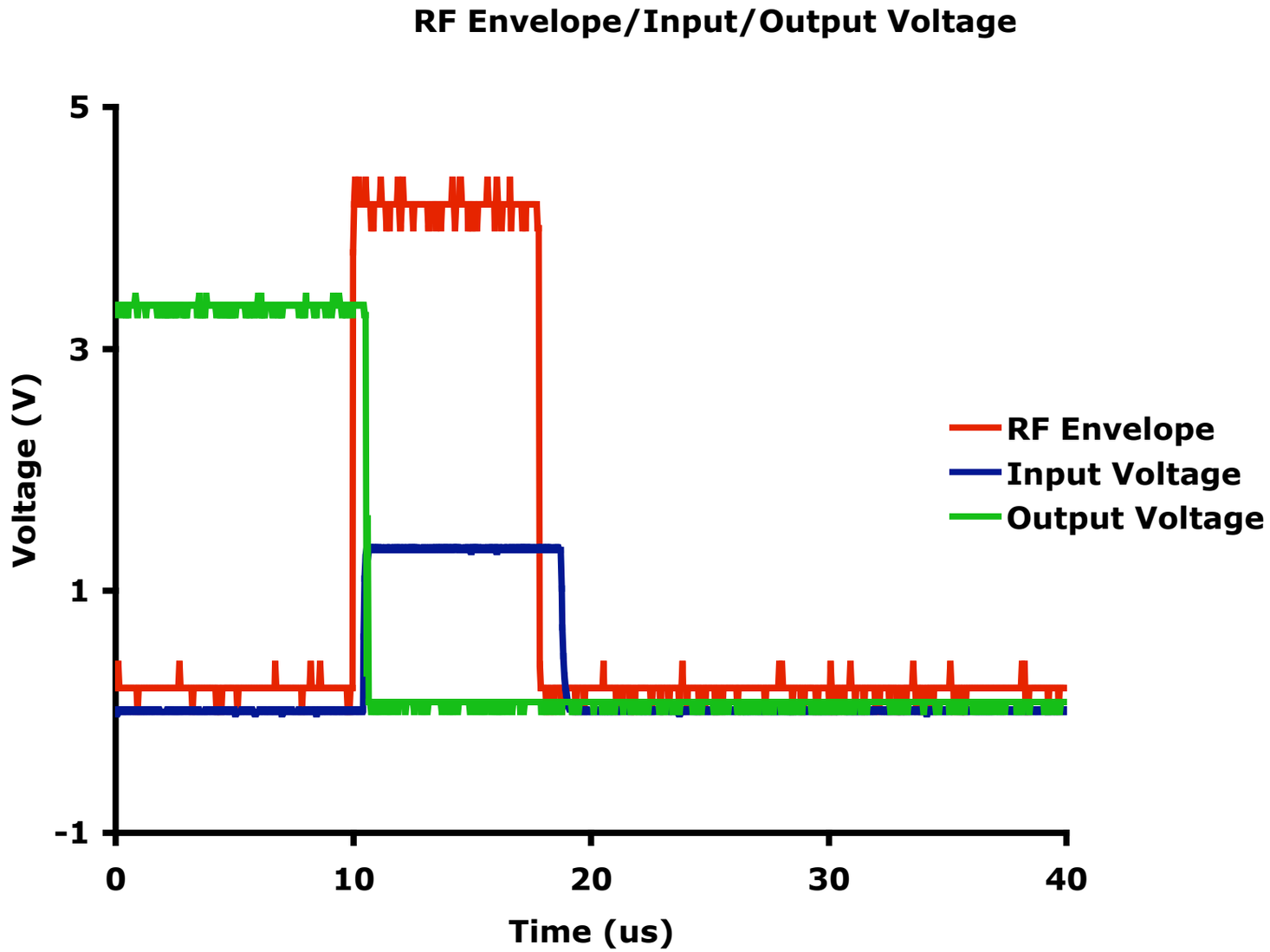

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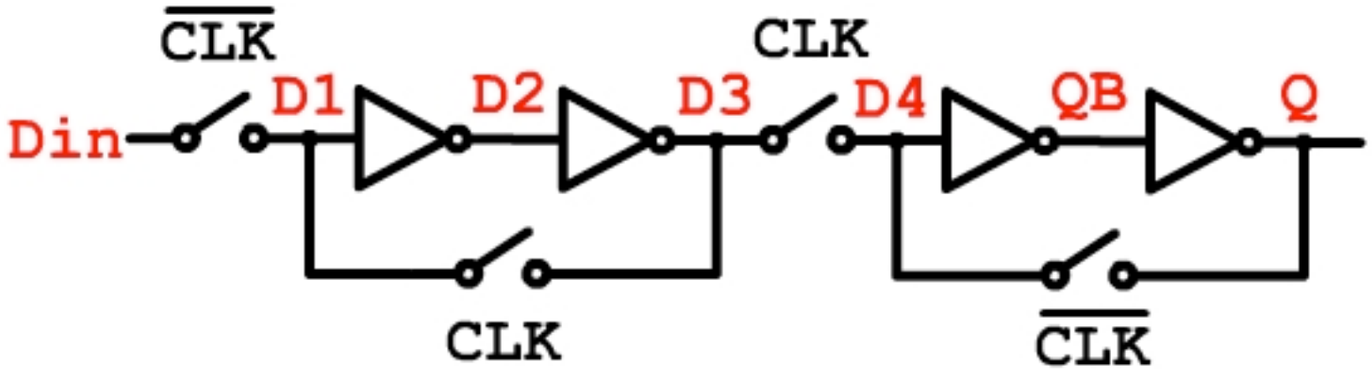
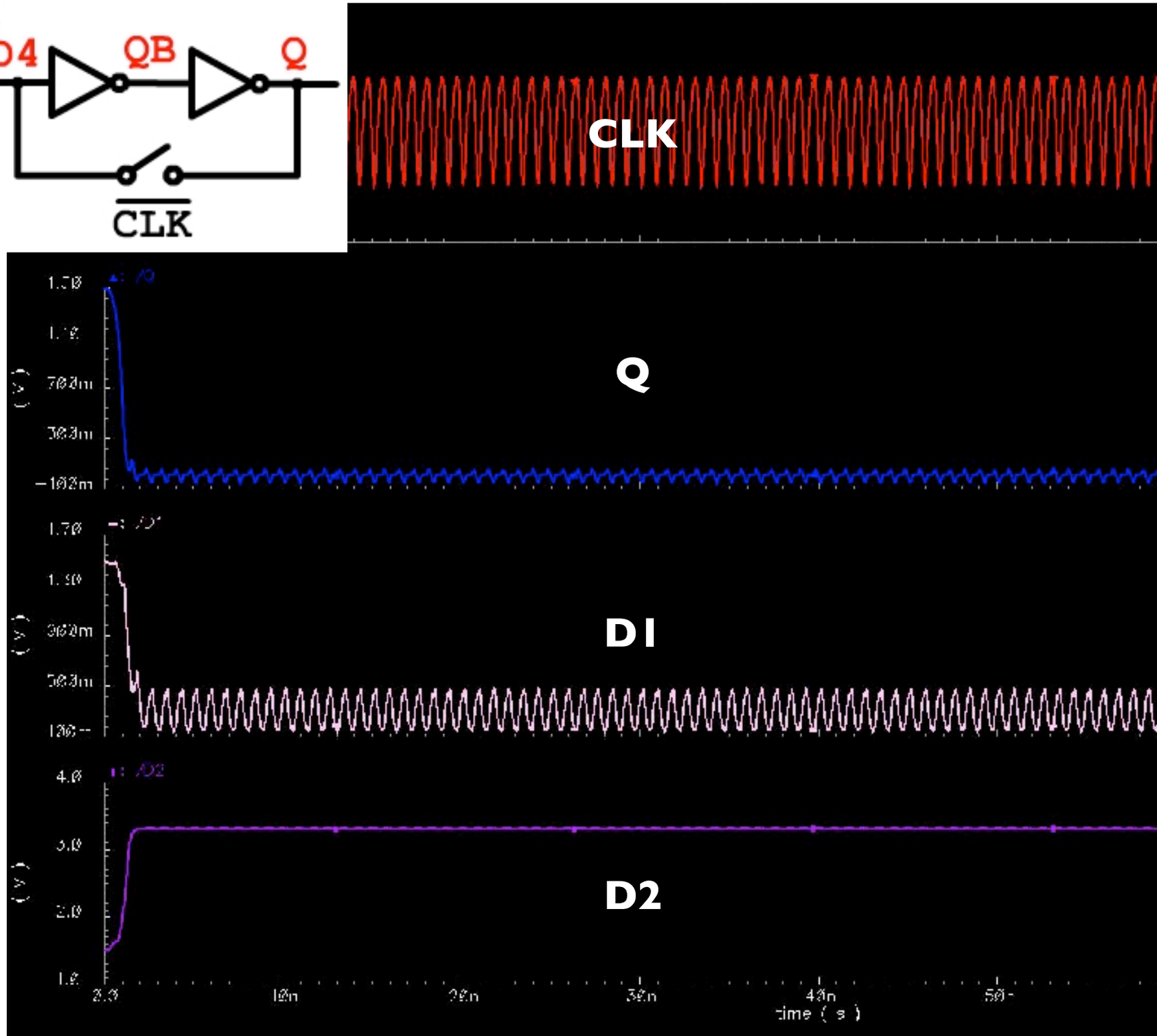


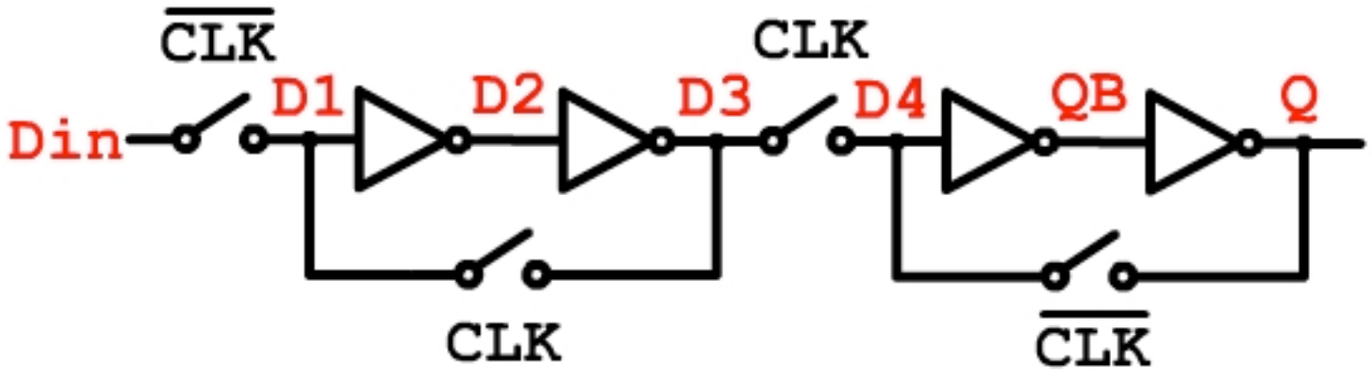
CLOCK INPUT

- Verification through SPICE simulation

1. Triggering
Only by Envelope



Recent Work



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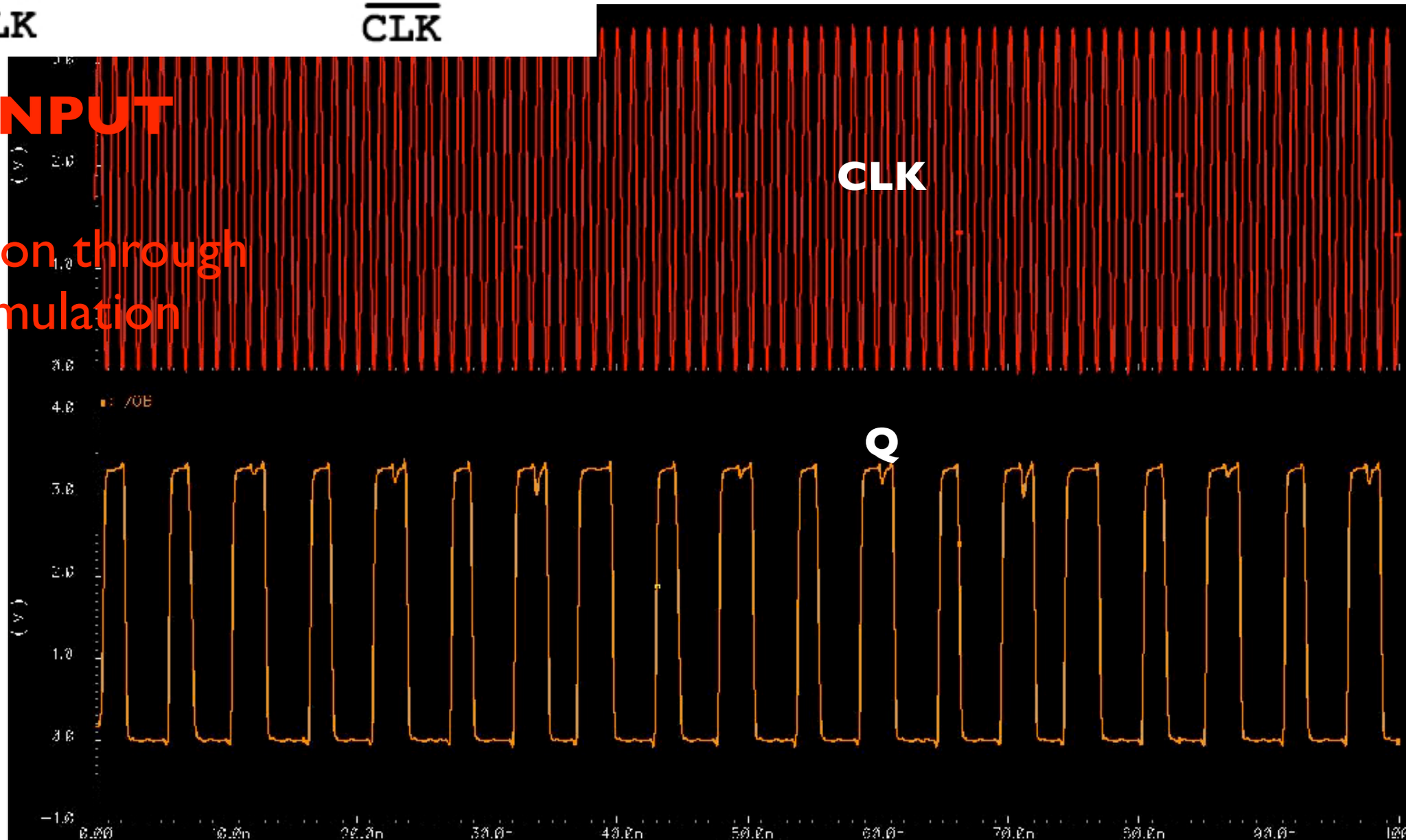
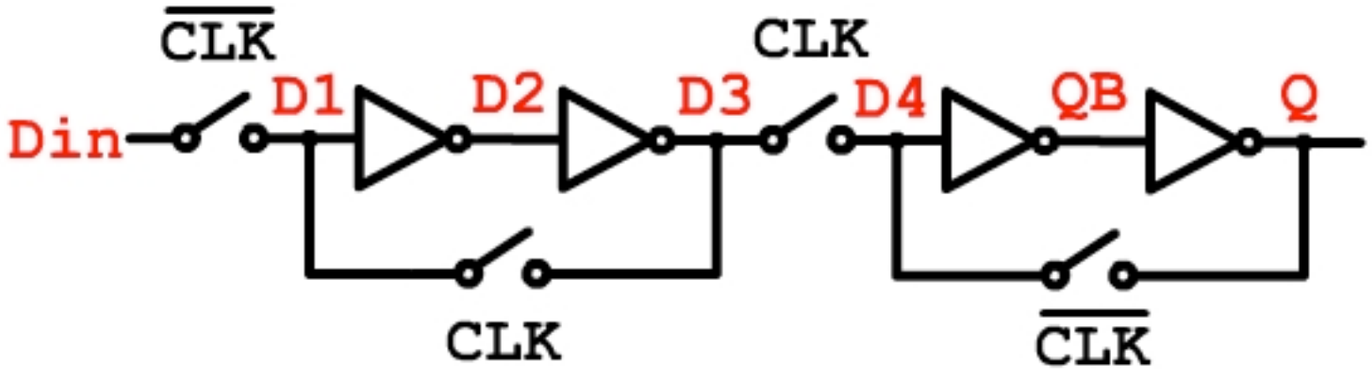


2. Aperiodic Triggering

Recent Work



CLOCK INPUT

- Verification through SPICE simulation

3. Periodic Metastability

Future Work

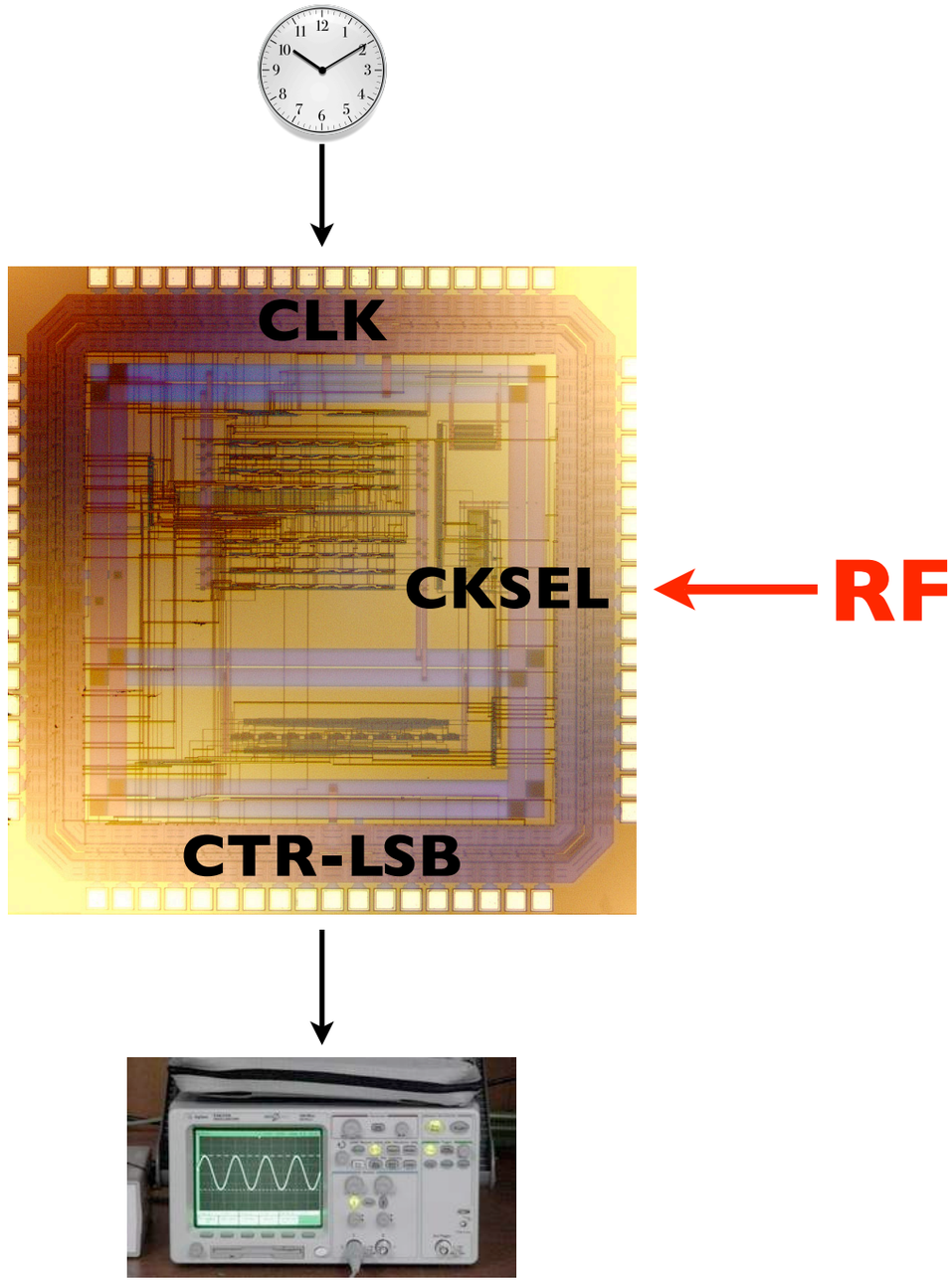
DATA INPUT/OUTPUT

- Measure the sensitivity of test-chip data pins

CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING



Future Work

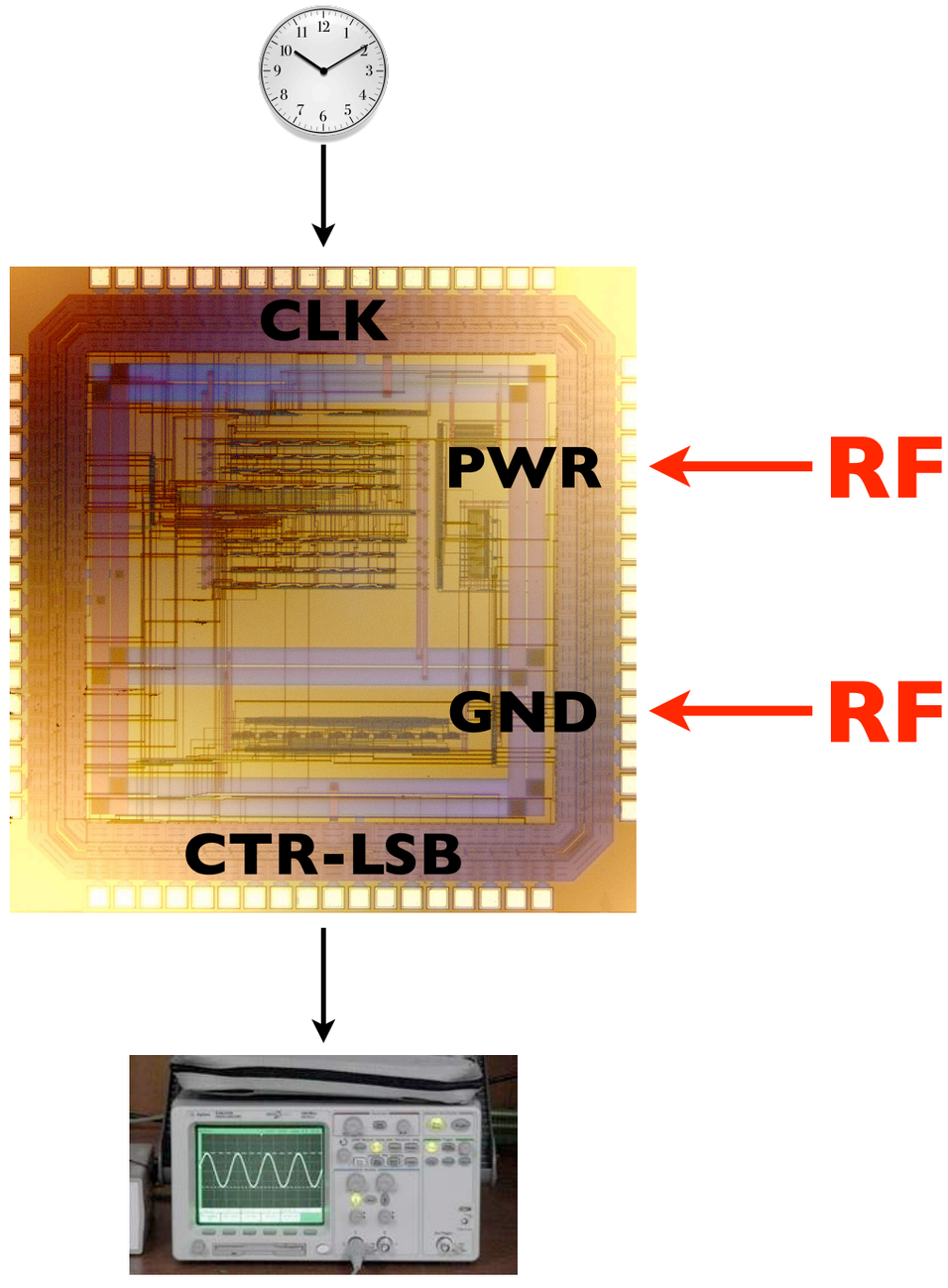
DATA INPUT/OUTPUT

CLOCK INPUT

GROUND PLANES

- Characterize levels for incorrect logic

ON-CHIP COUPLING



Future Work

DATA INPUT/OUTPUT

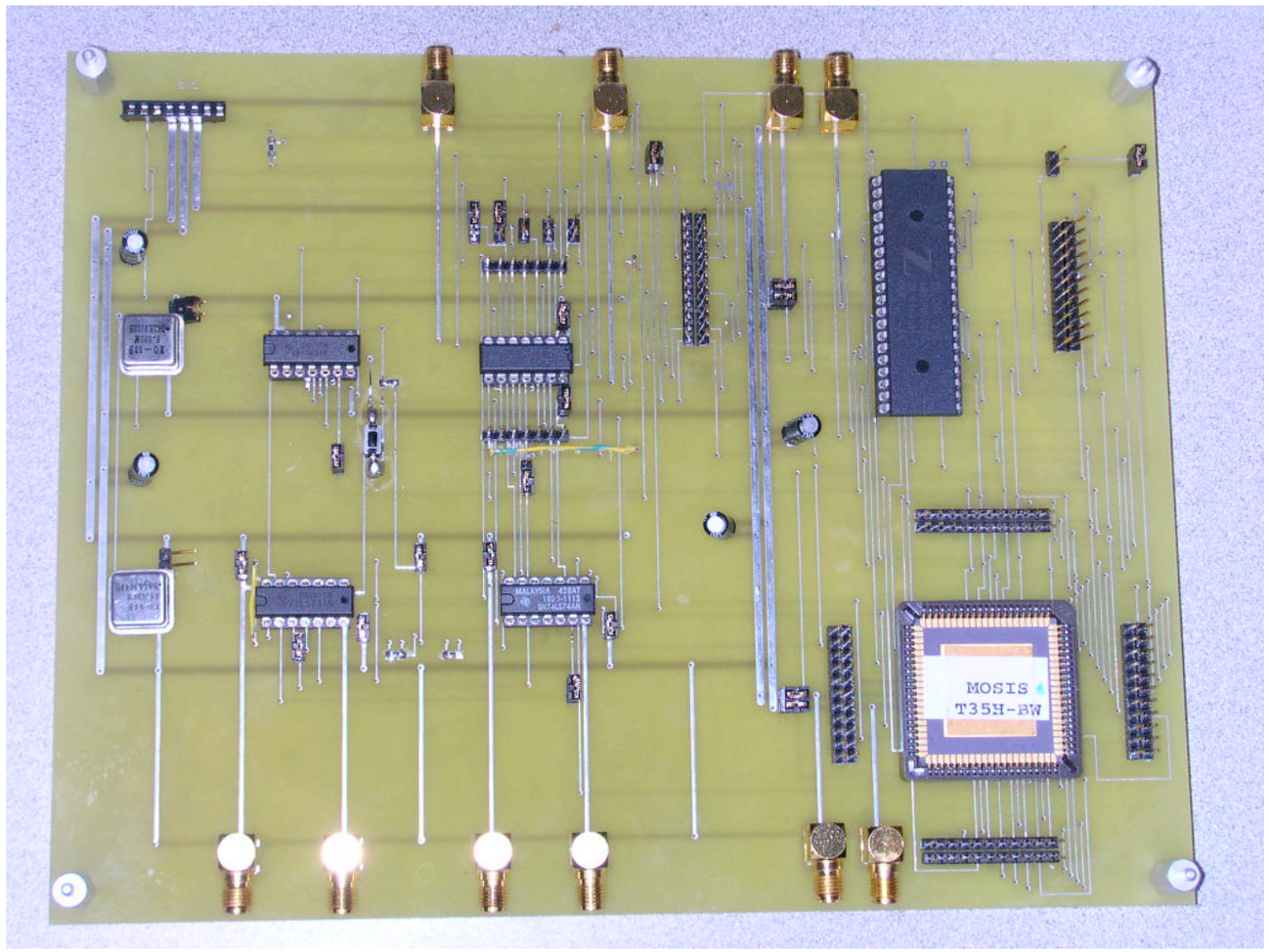
CLOCK INPUT

GROUND PLANES

- Measure RF levels that disrupt comm.

ON-CHIP COUPLING

Experimental PCB to test
RF disruption of chip-chip signaling



Future Work

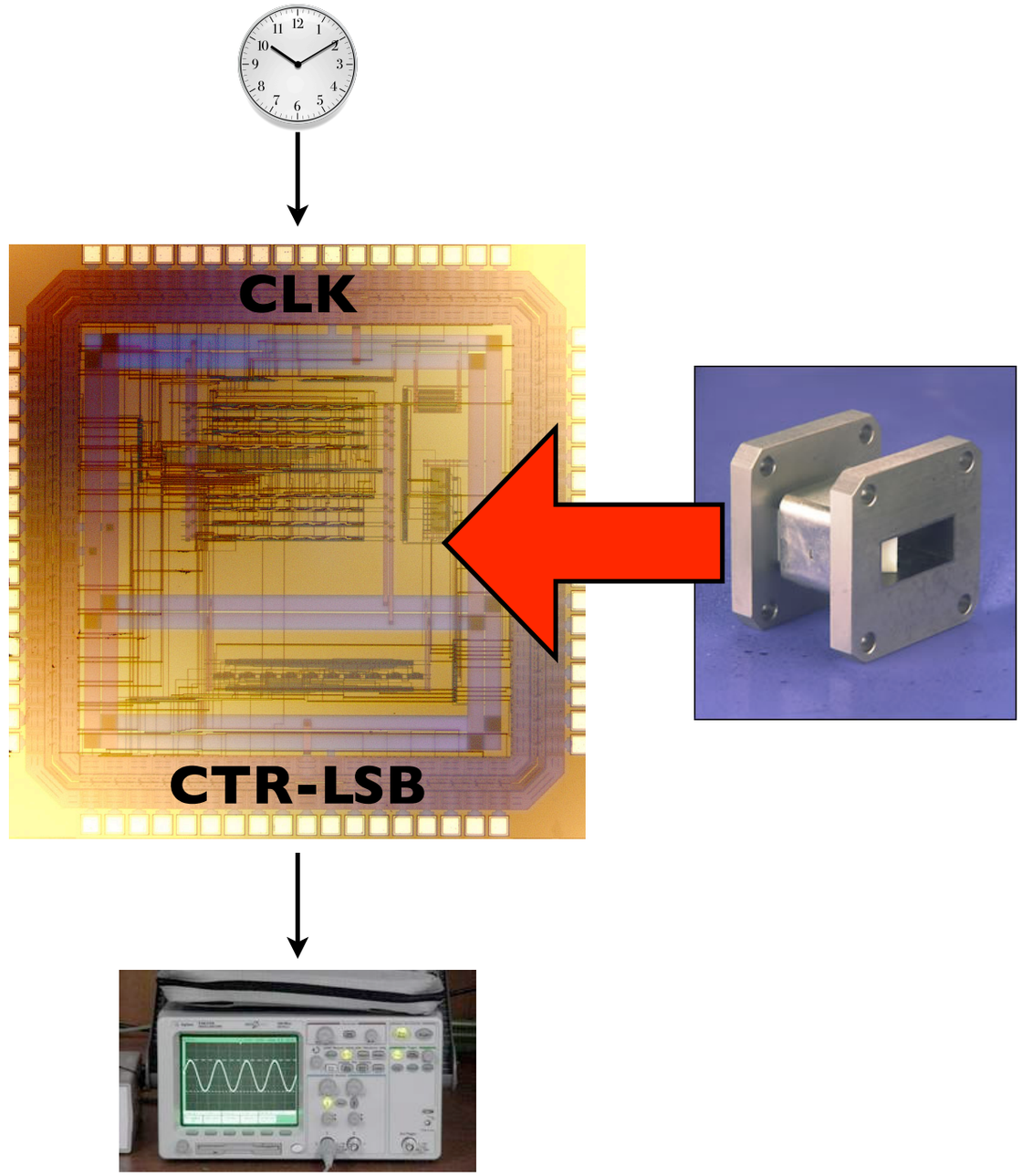
DATA INPUT/OUTPUT

CLOCK INPUT

GROUND PLANES

ON-CHIP COUPLING

- Characterize the level of coupling to on-die structures



Acknowledgments

GRAD STUDENTS:

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INVALUABLE AID:

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